10- control gate
11- floating gate
22- shallow junction
33- deep junction
34- lightly doped n-
44- p+ implant
14- ONO
15- tunnel oxide
16- p-substrate
48- edge erase
49- CHE program

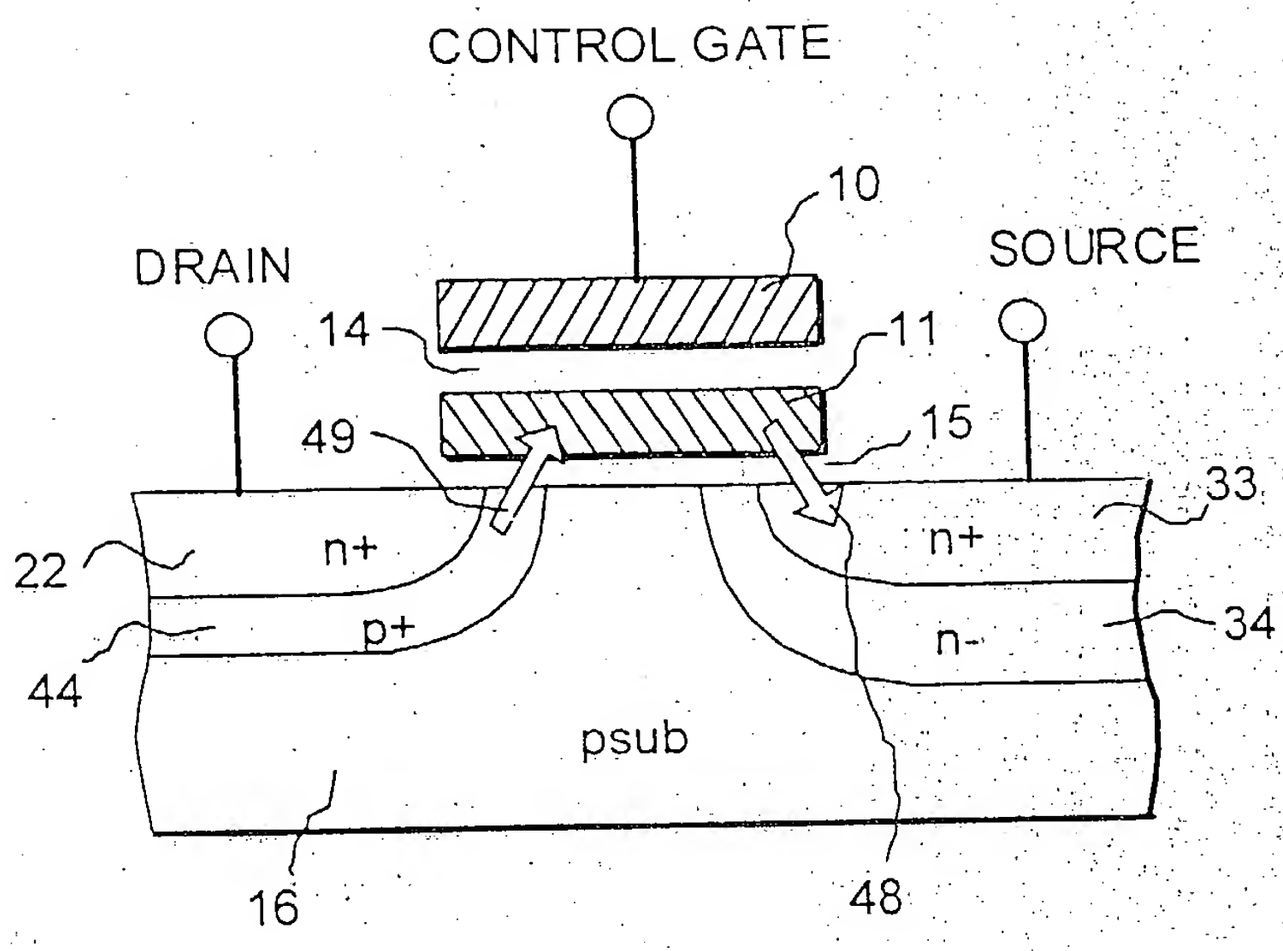


FIG.1 (Prior Art)

10- control gate
11- floating gate
22- shallow junction
13- shallow junction
44- p+ implant
14- ONO
15- tunnel oxide
16- p-substrate
38- channel erase
49- CHE program

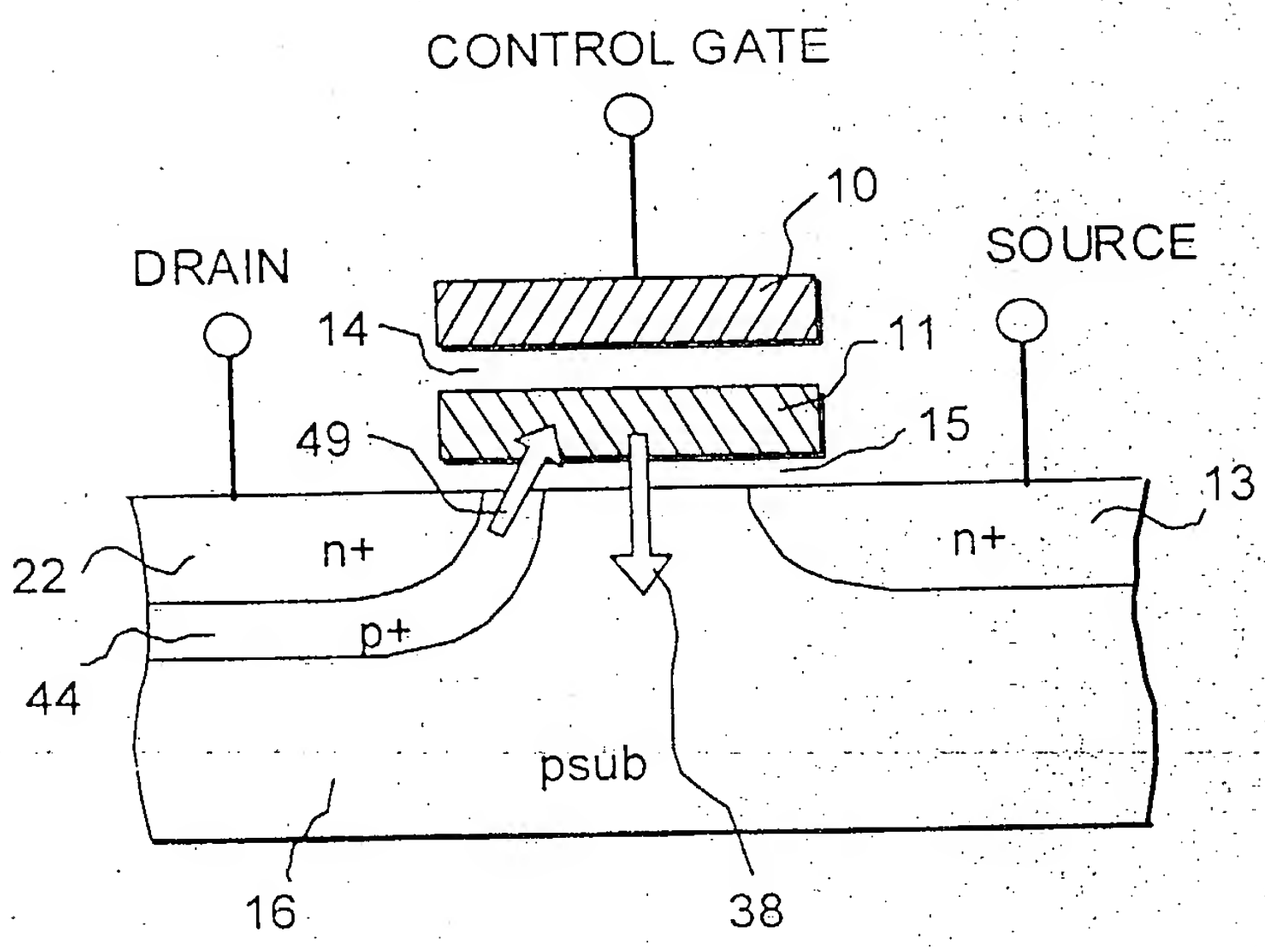


FIG.2(Prior Art)

10- control gate
11- floating gate
12- deep junction
20- lightly doped n-
13- shallow junction
14- ONO
15- tunnel oxide
16- p-substrate
17- p+ implant
18- channel erase
19- edge program

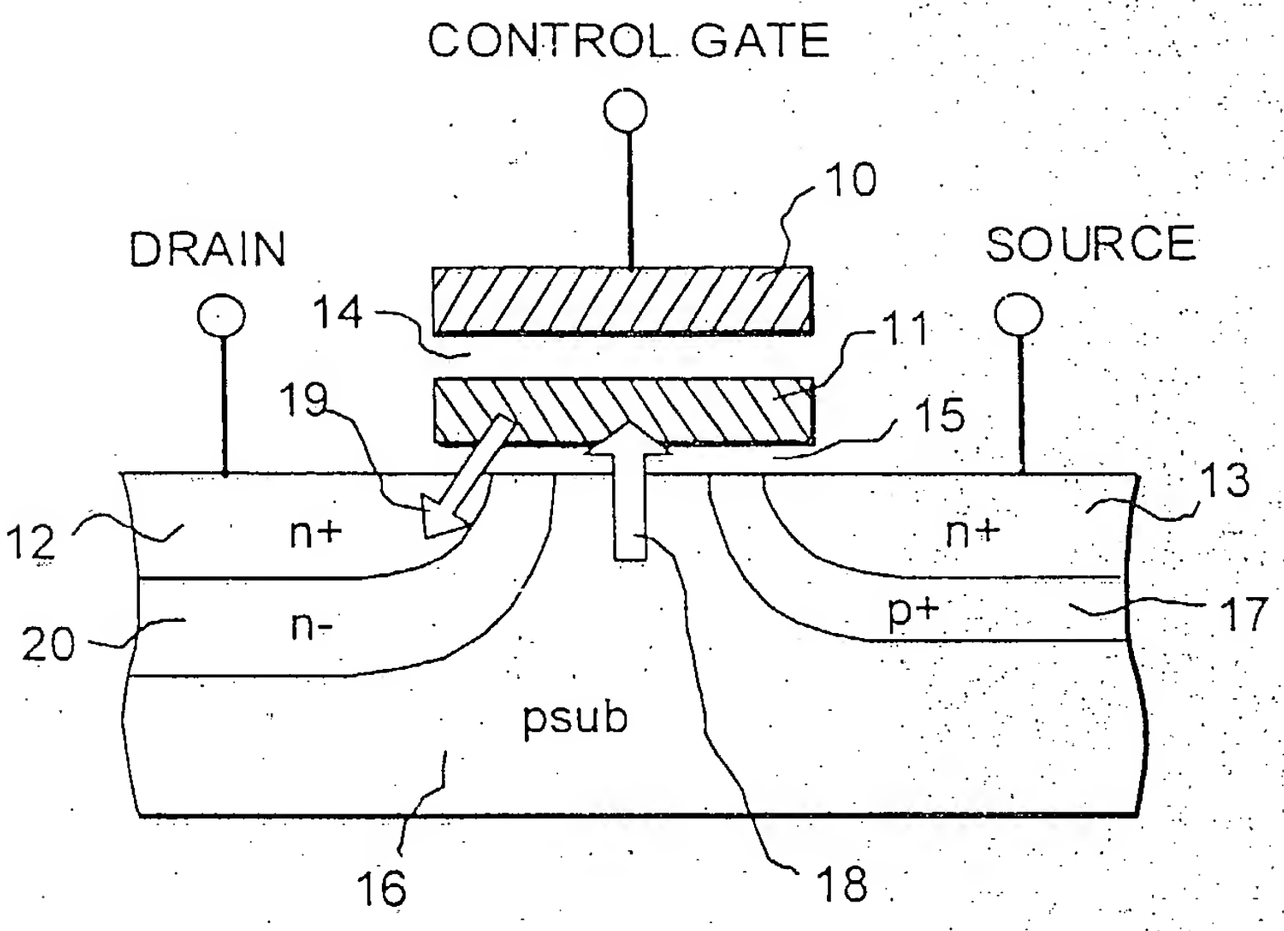


FIG.3 (Prior Art)

10- control gate
11- floating gate
22- shallow junction
13- shallow junction
14- ONO
15- tunnel oxide
16- p-substrate
27- channel erase
28- channel program

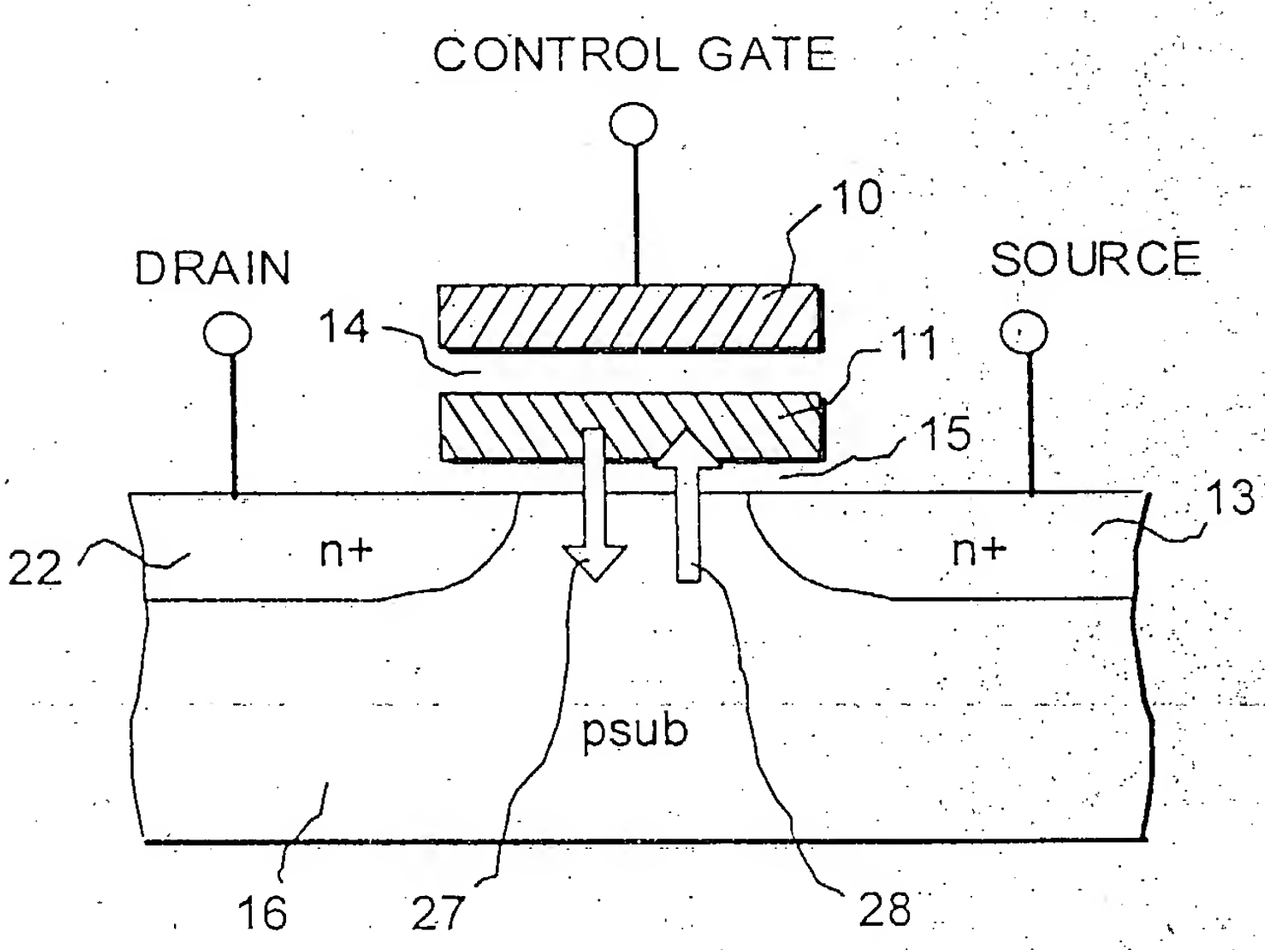
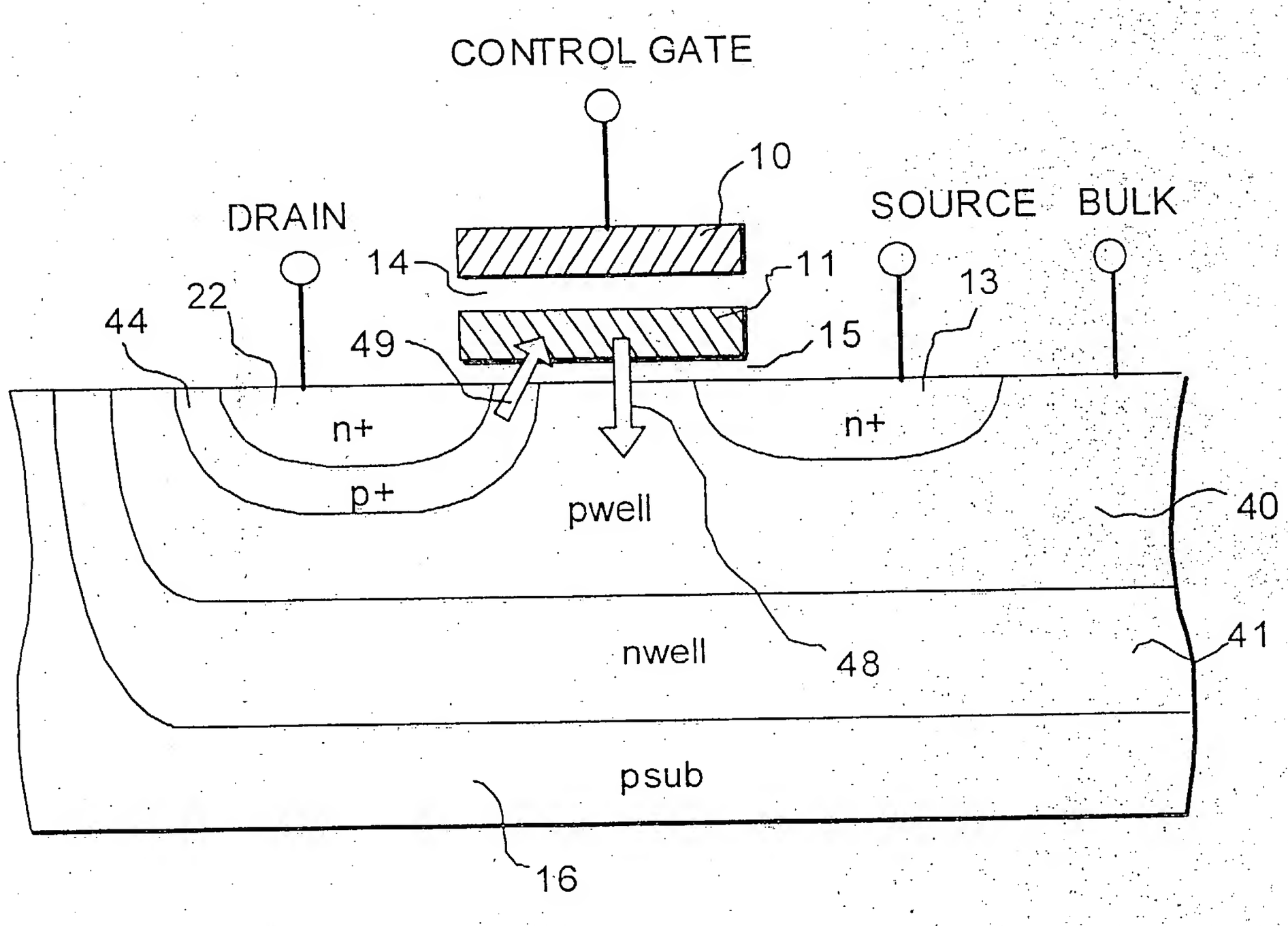


FIG.4 (Prior Art)



10- control gate
11- floating gate
22- shallow junction
13- shallow junction
44- p+ implant
14- ONO
15- tunnel oxide
38- channel erase
49- CHE program
40- p-well
41- deep n-well
16- p-substrate

FIG.5 (Prior Art)

ETOX NOR Cell on a P-substrate

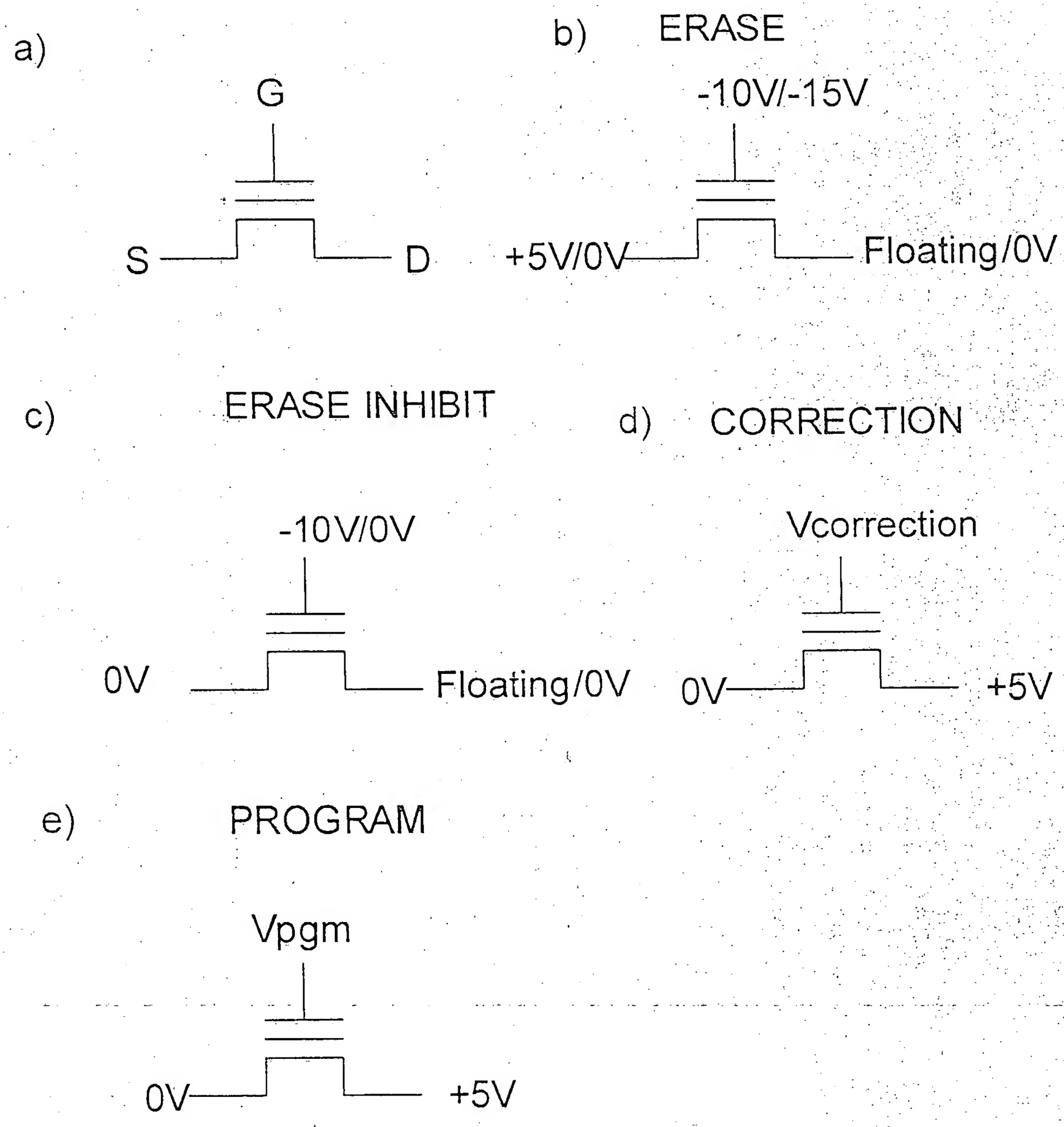
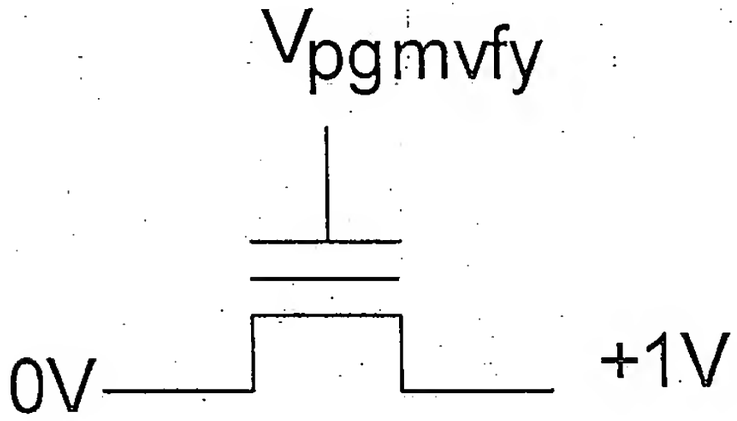


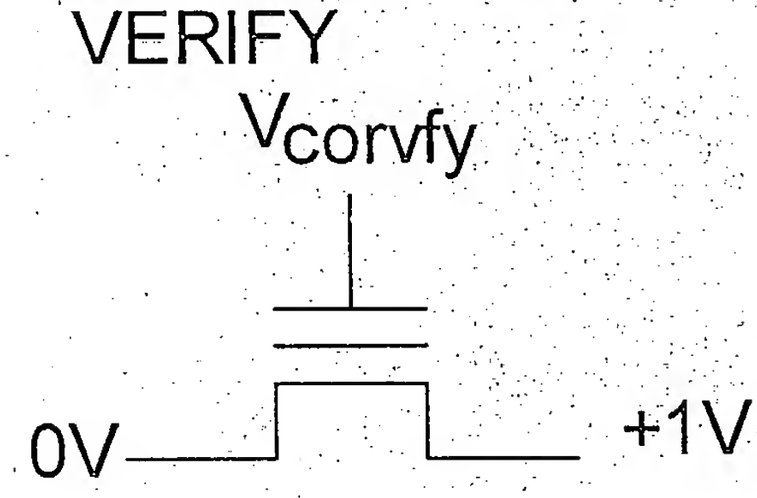
FIG. 6

ETOX NOR Cell on a P-substrate

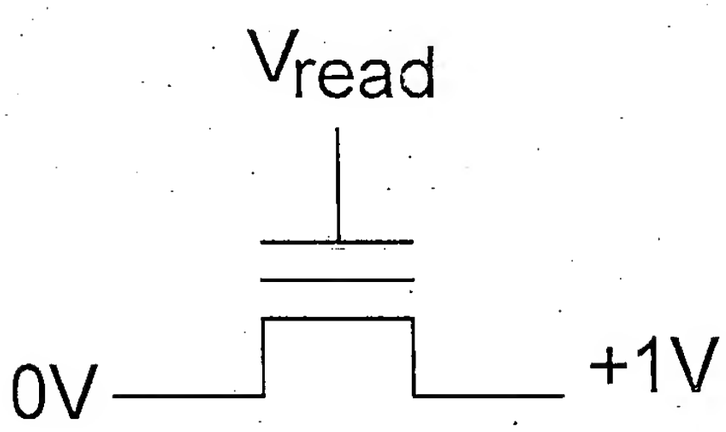
a) PROGRAM VERIFY



b) CORRECTION VERIFY



c) READ



d) ERASE VERIFY

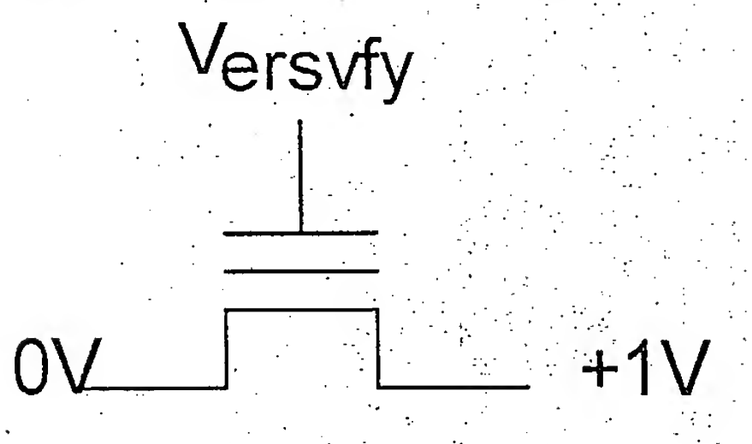


FIG. 7

ETOX NOR Cell on a P-substrate

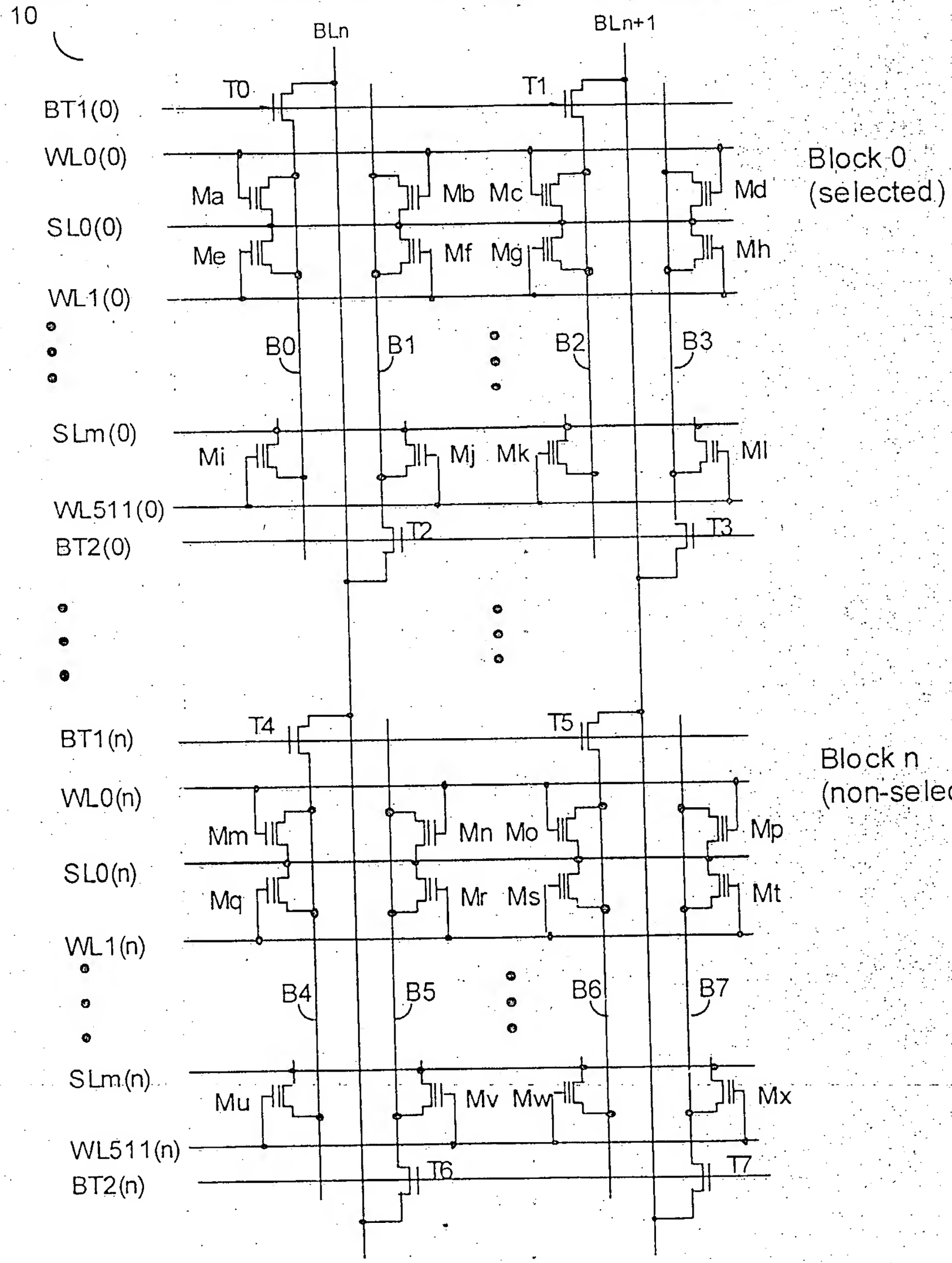


FIG.8

Block Erase Operations

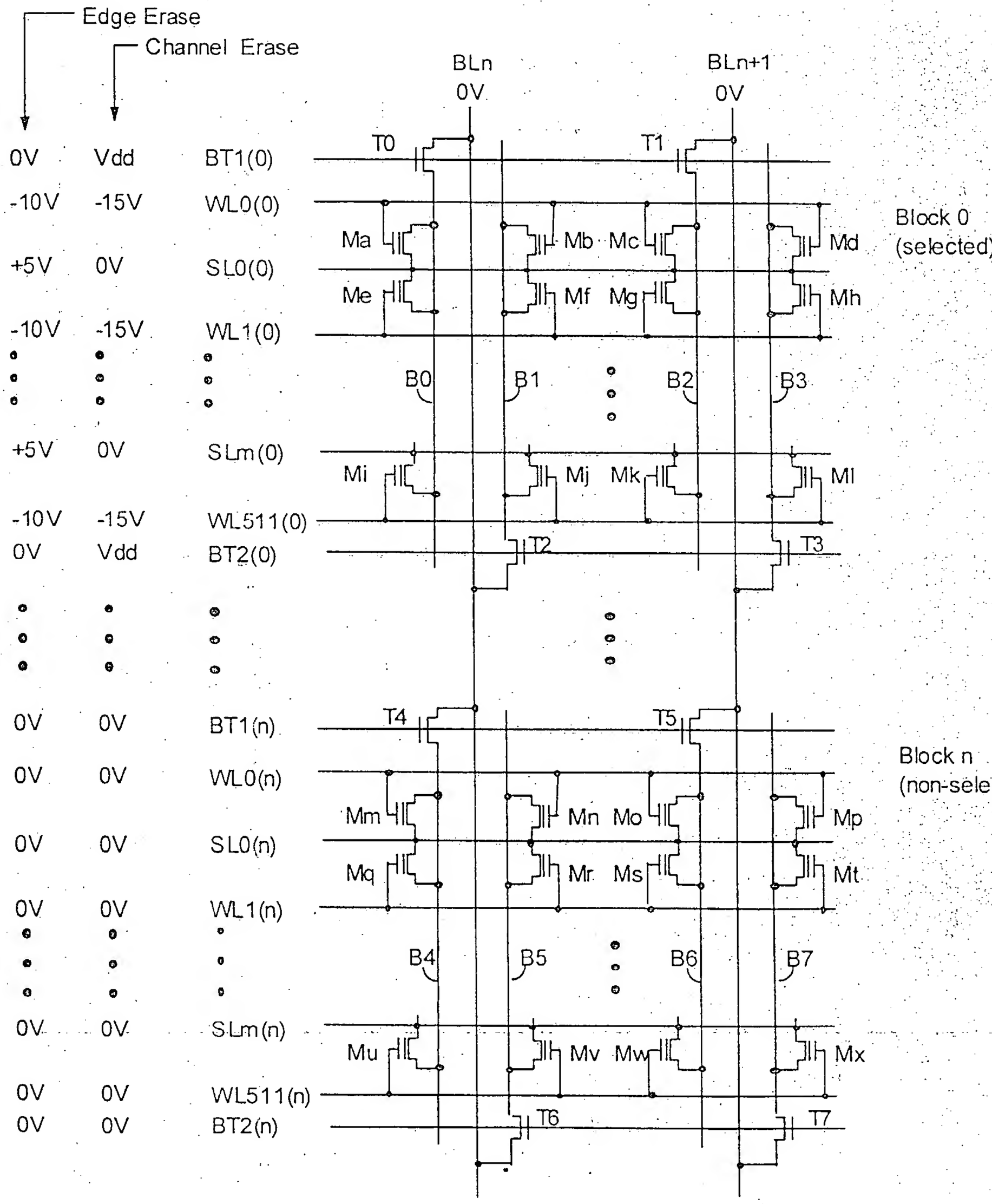


FIG. 9

Block Erase Verify

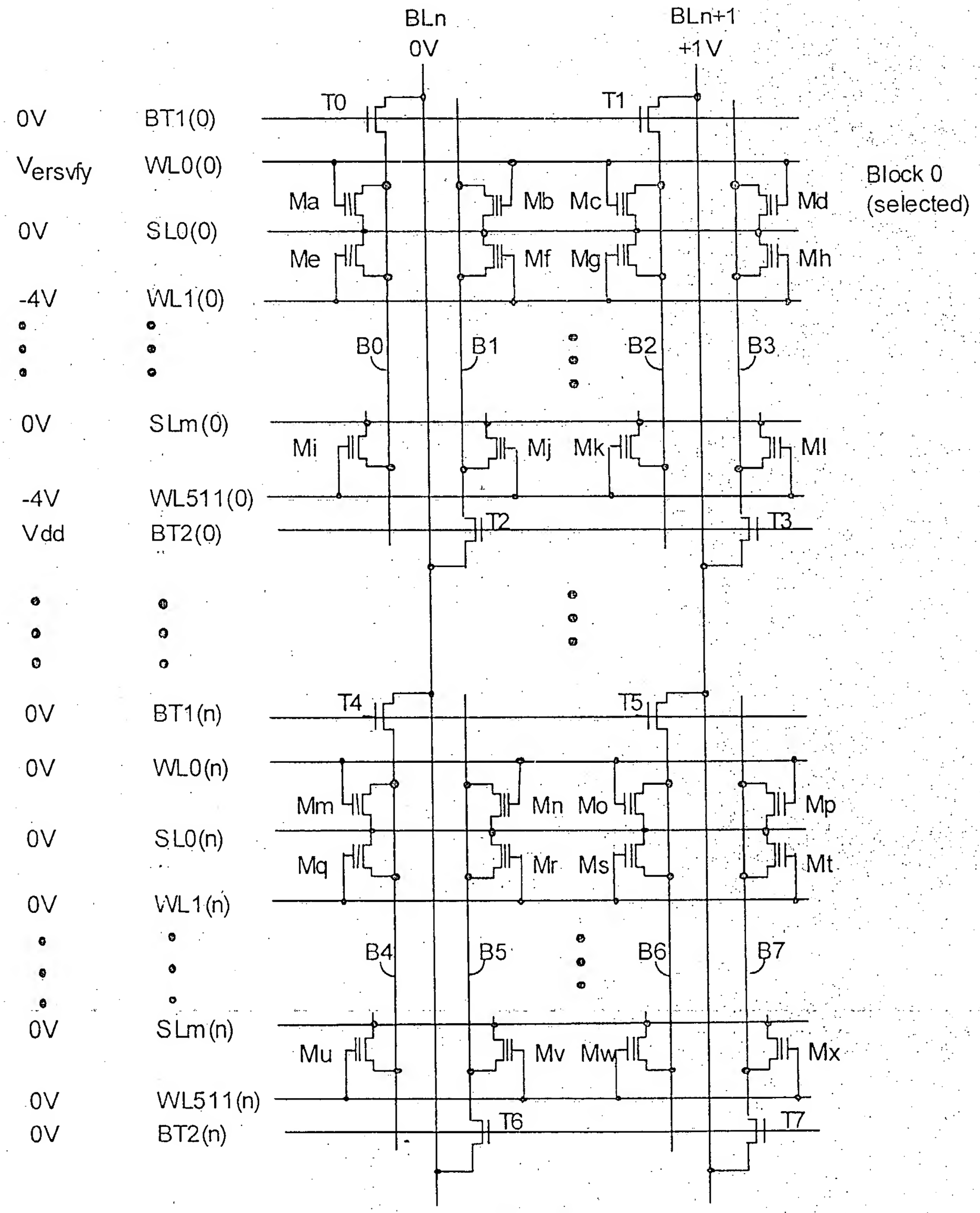


FIG.10

Erase Inhibit

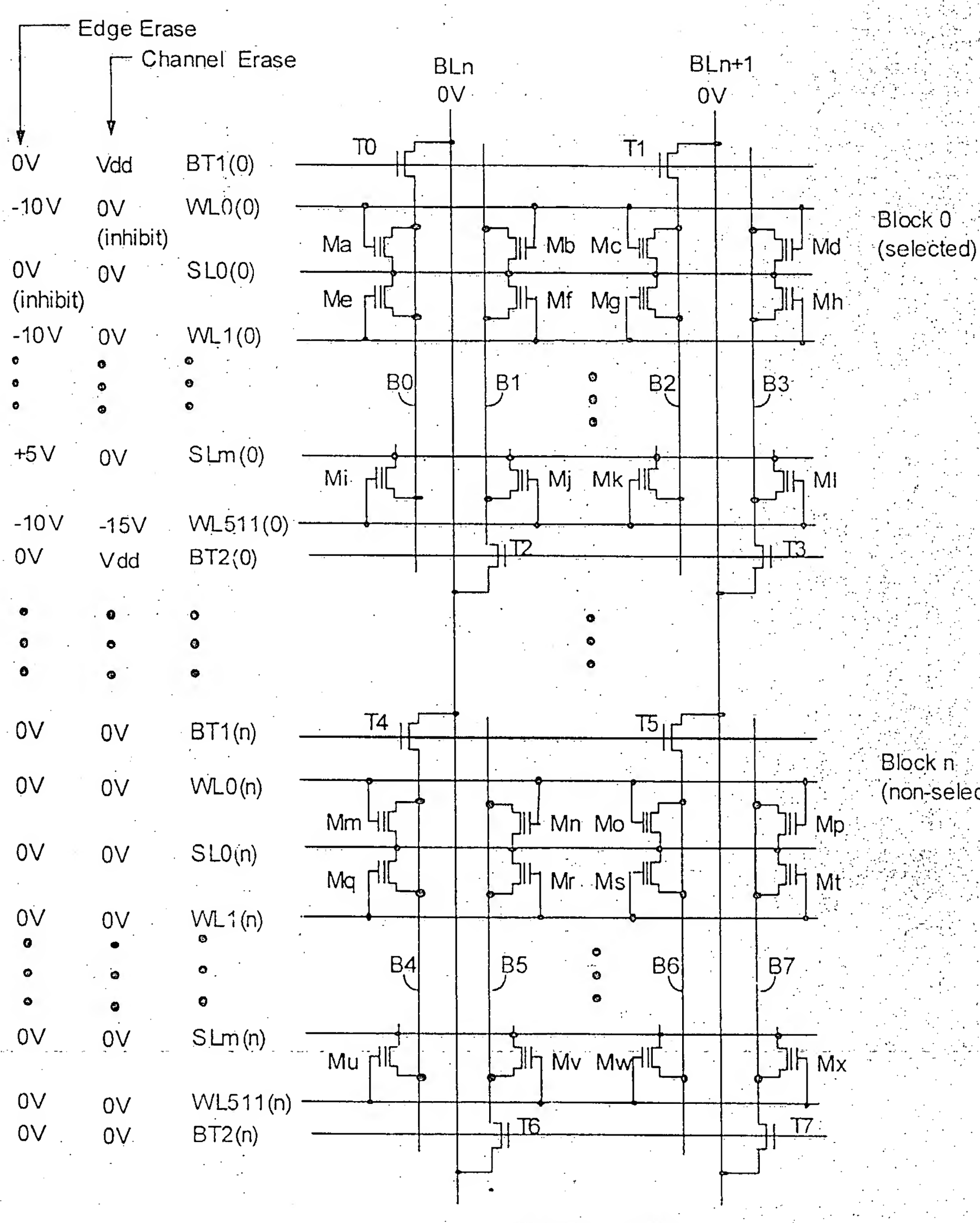


FIG. 11

Correction Operations

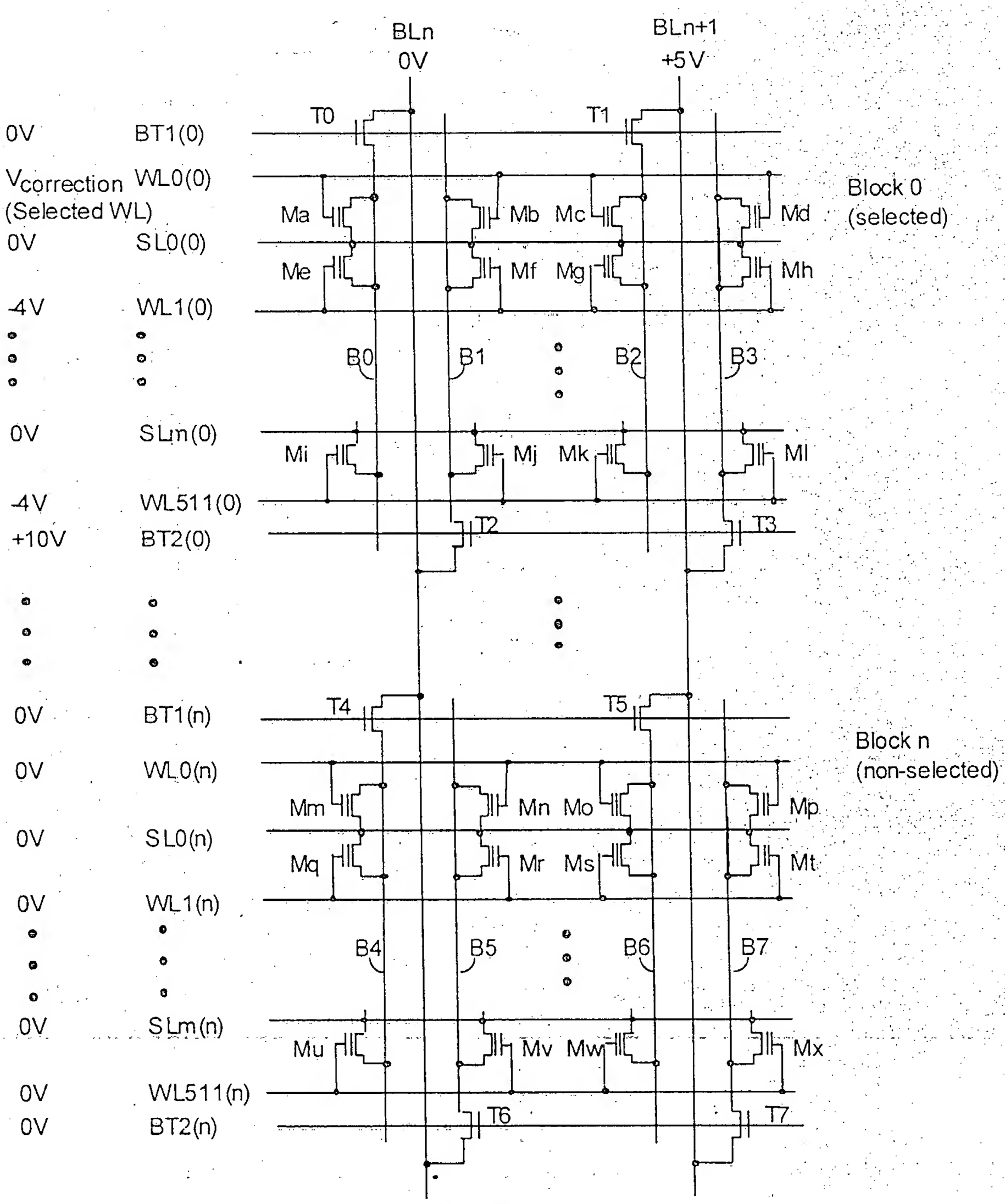


FIG. 12

Correction Verify Operations

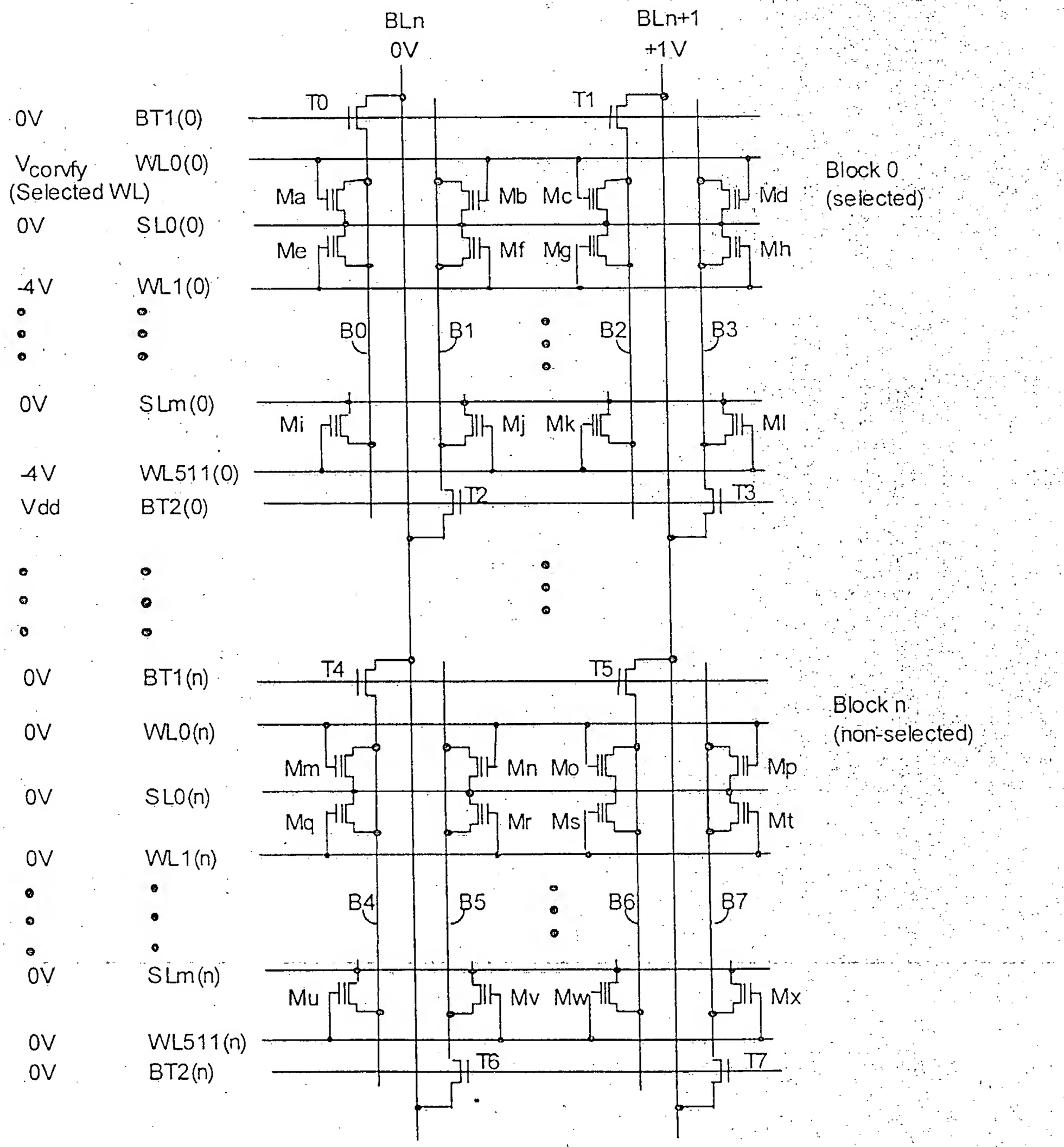


FIG. 13

Program Operations

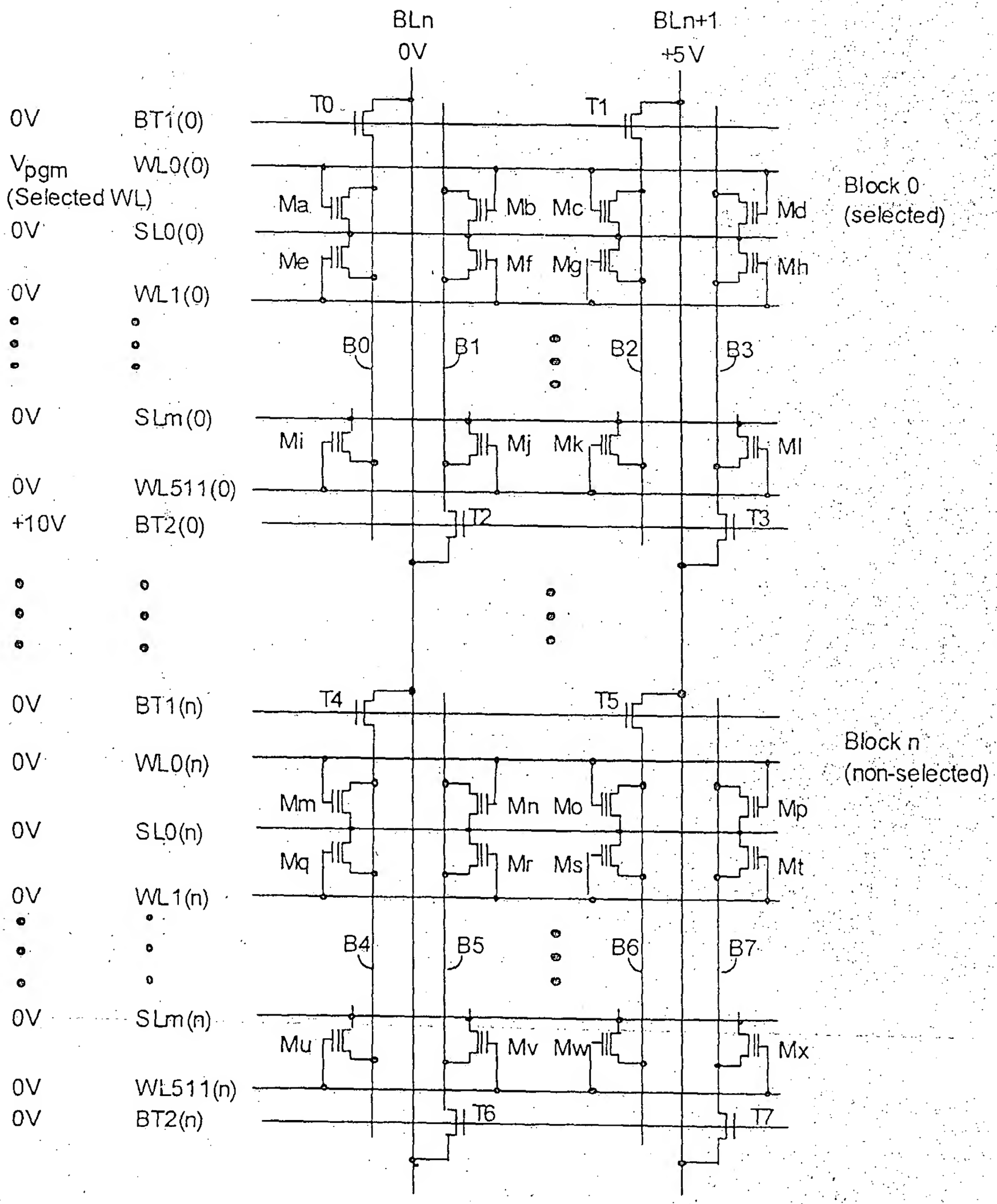


FIG. 14

Program Verify Operations

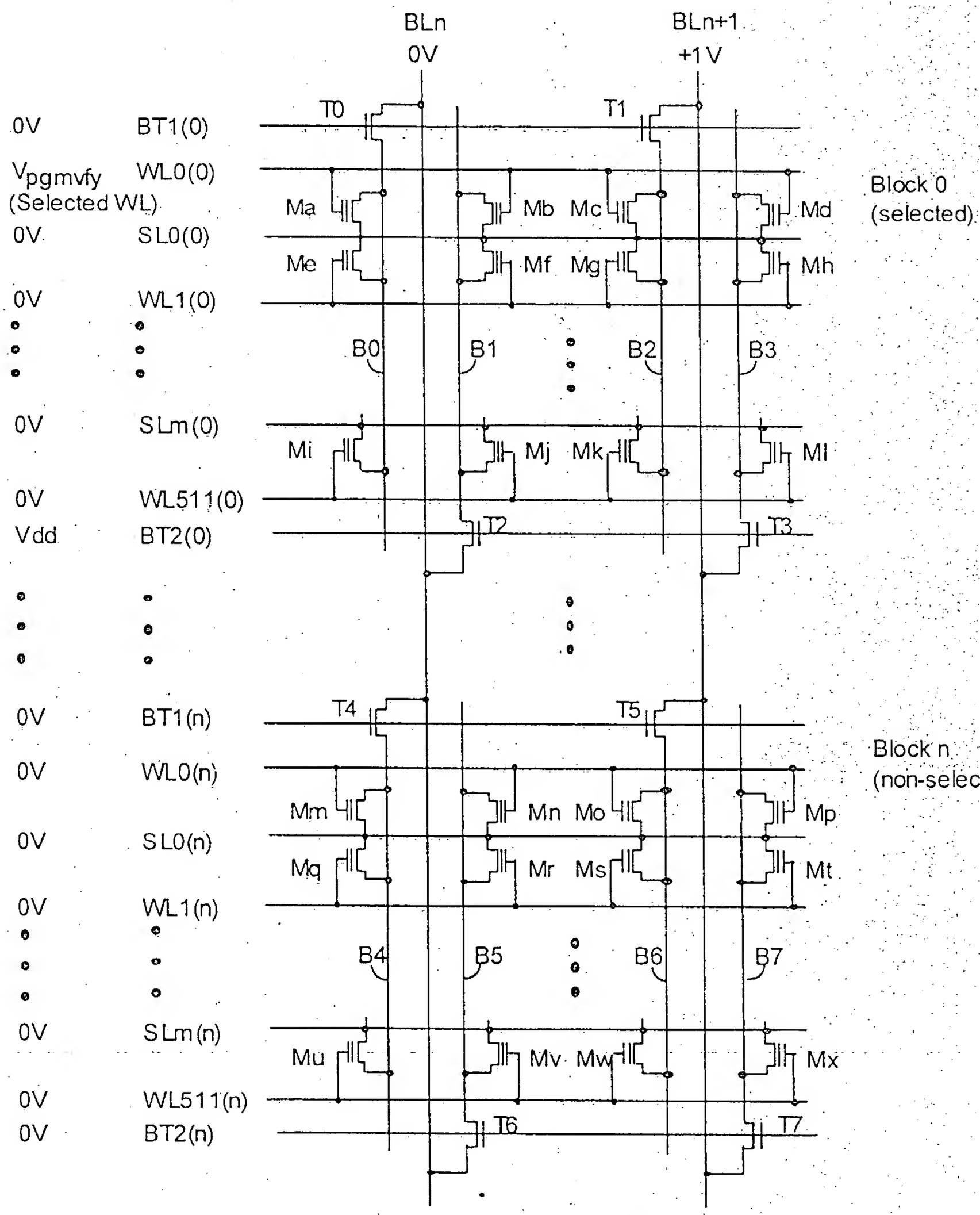


FIG. 15

Cell on a P-substrate for this invention

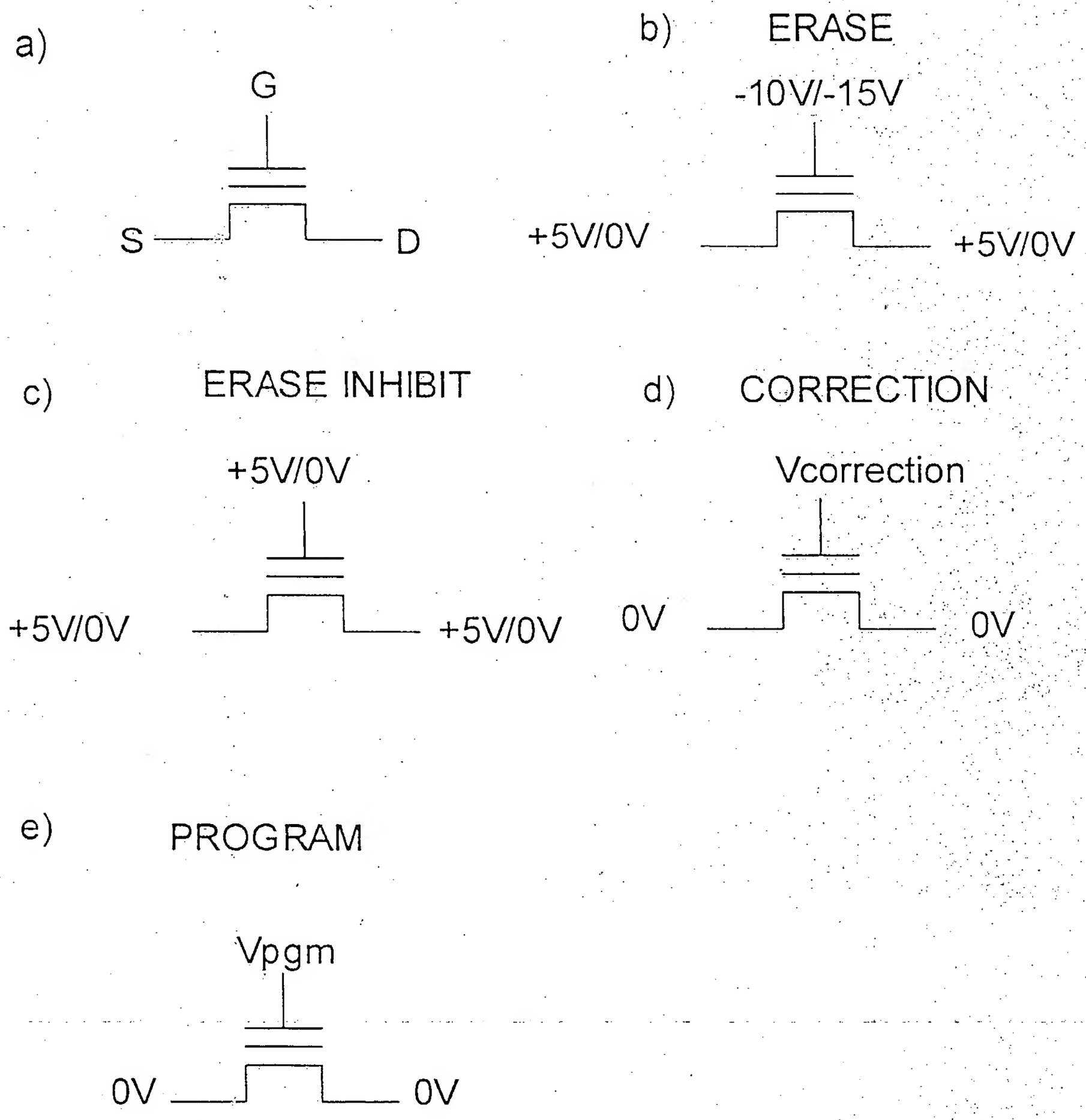
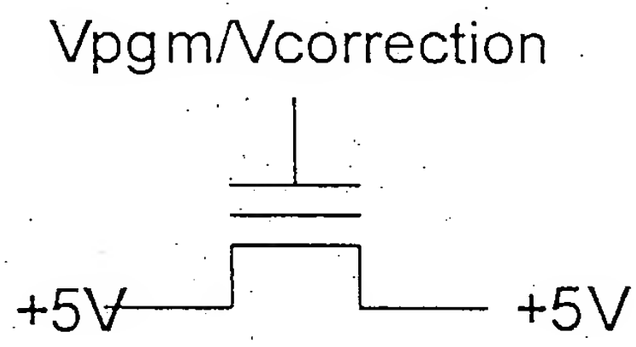


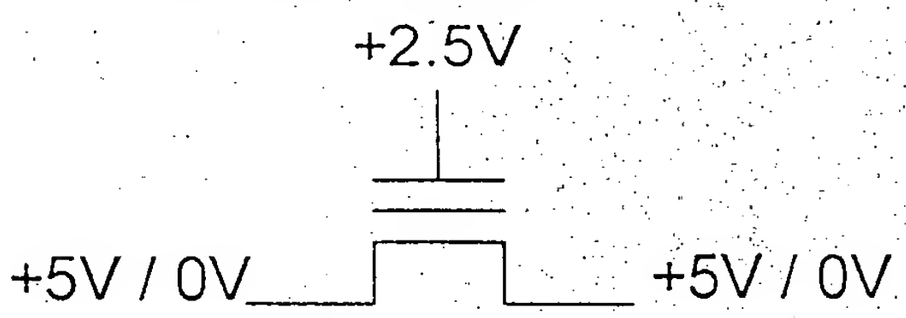
FIG. 16

Cell on a P-substrate for this invention

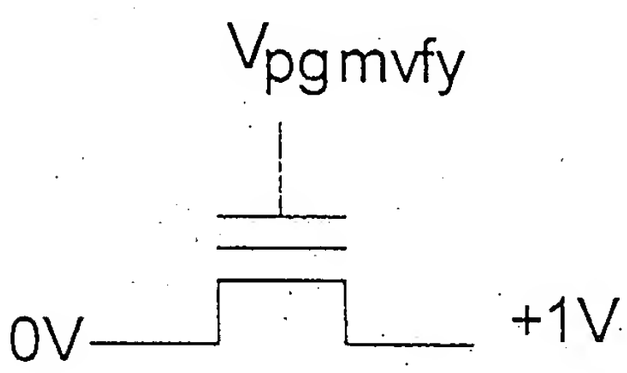
a) PROGRAM/CORRECTION INHIBIT
(In same WL, in selected Block)



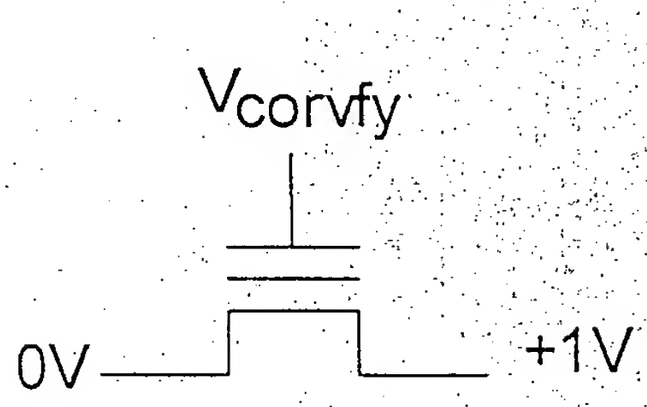
b) PROGRAM/CORRECTION INHIBIT
(In different WL, in selected Block)



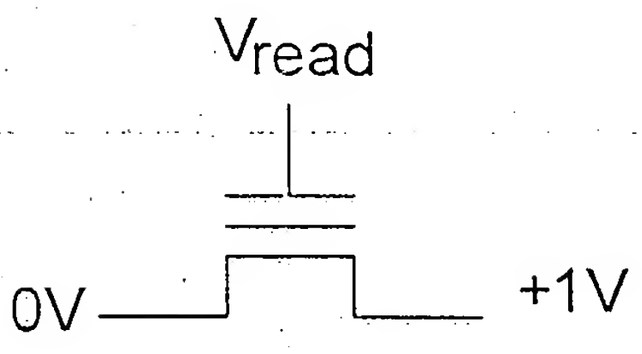
c) PROGRAM VERIFY



d) CORRECTION VERIFY



e) READ



f) ERASE VERIFY

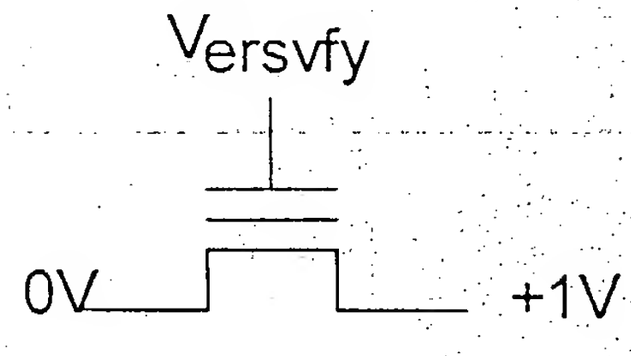


FIG. 17

AND Array on a P-substrate

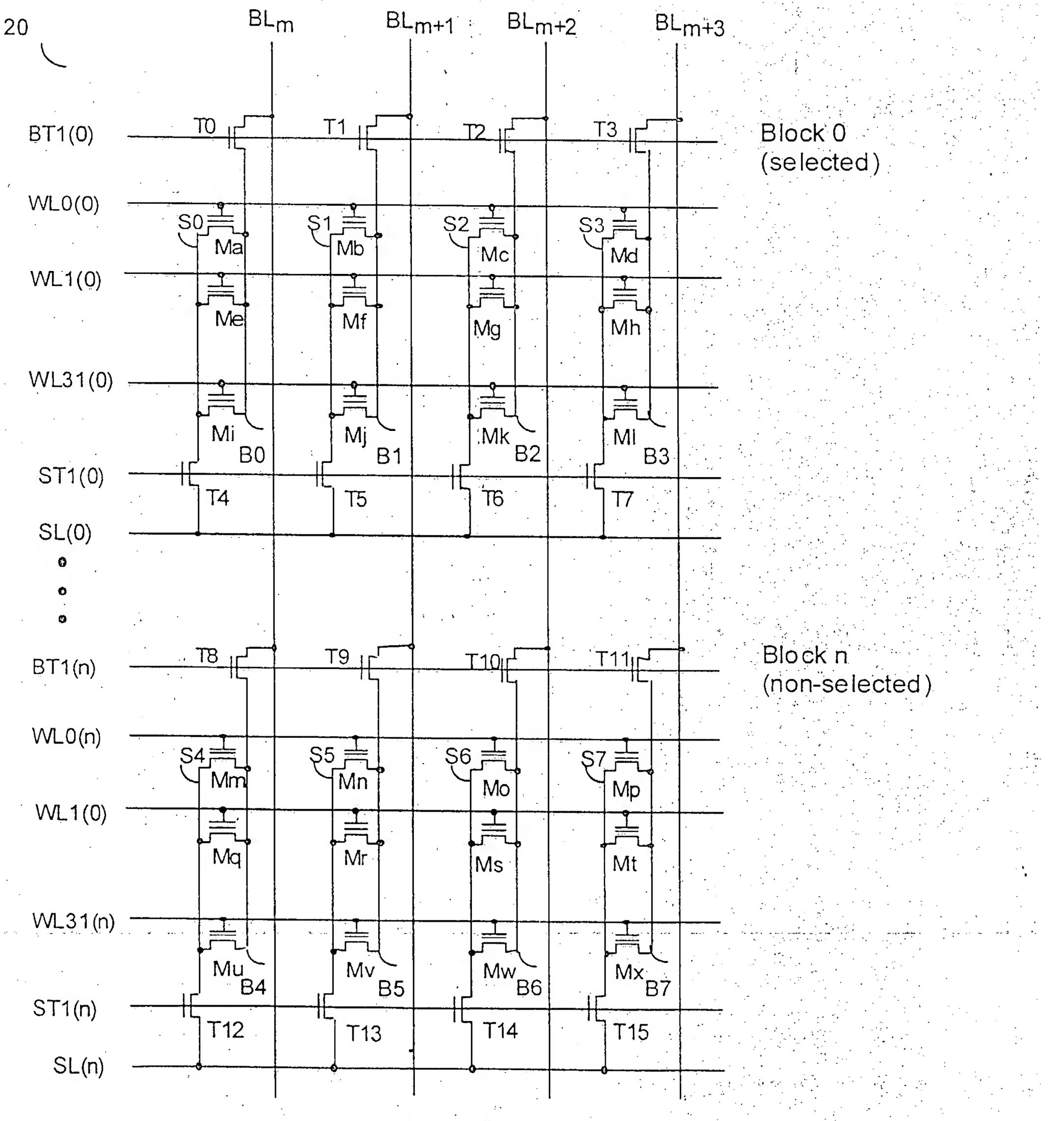


FIG. 18

Random Page Erase Operation

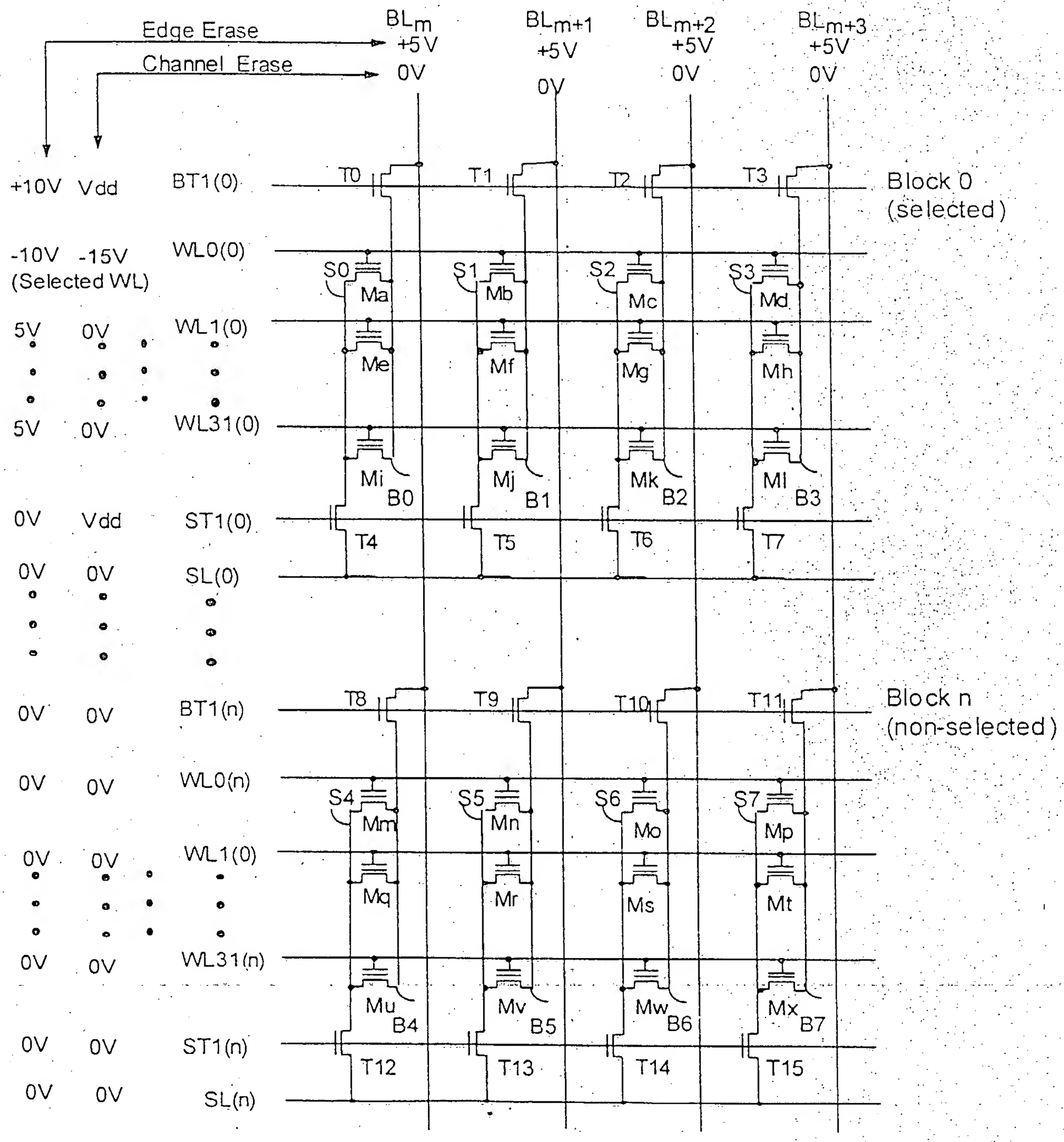


FIG.19

Random Page Erase Verify Operation

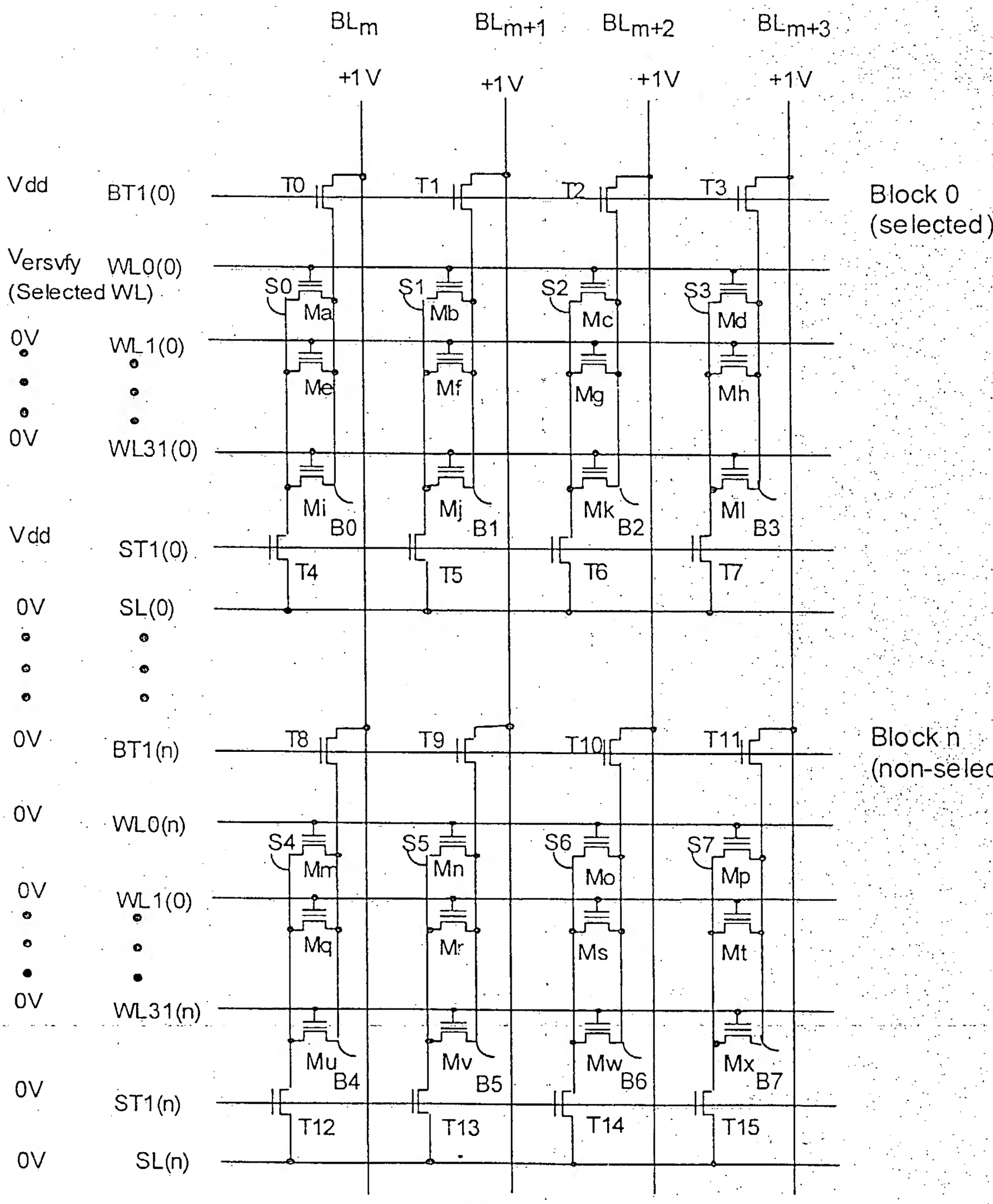


FIG. 20

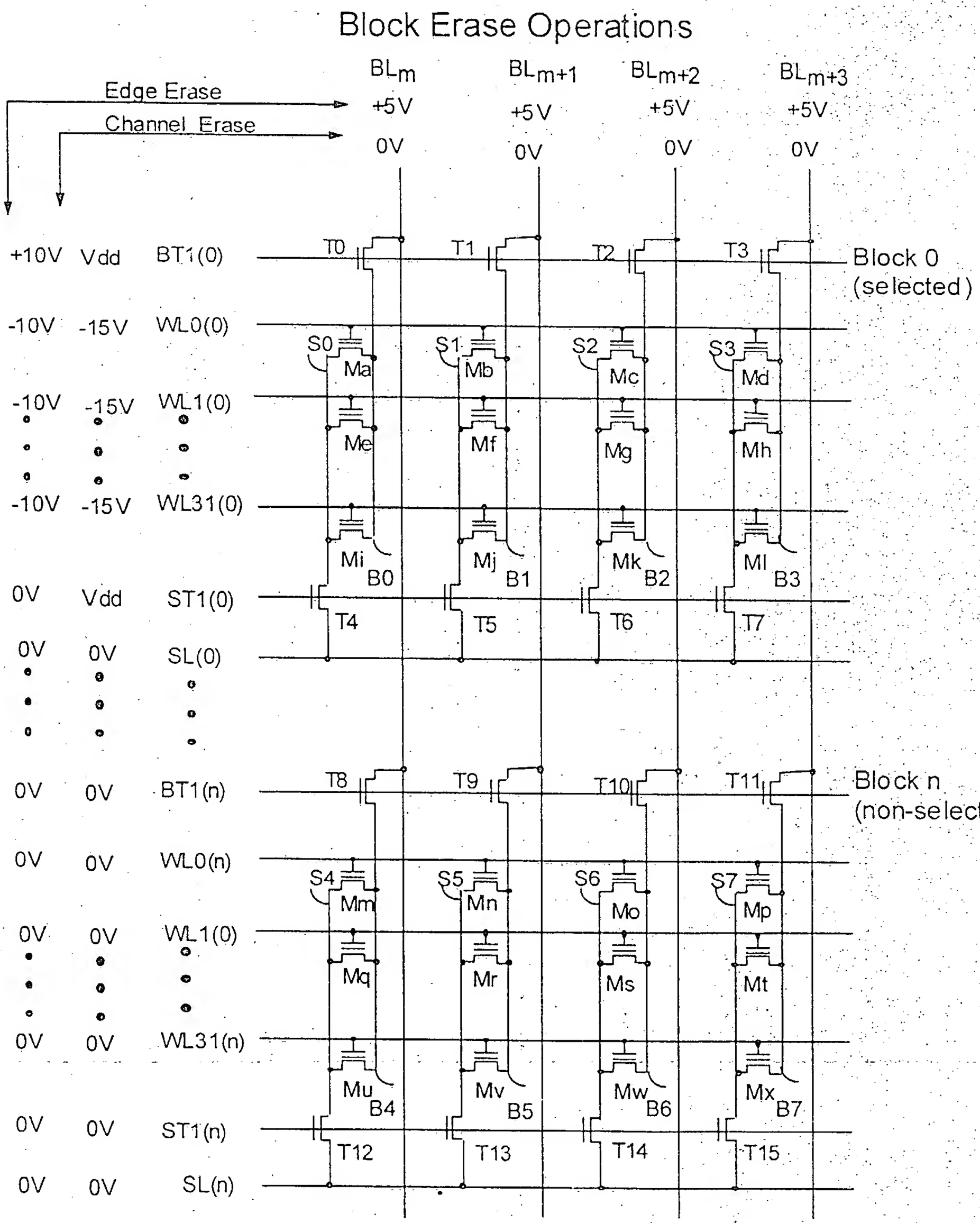

Block Erase Operations
BLm
BLm+1
BLm+2
BLm+3
Edge Erase
Channel Erase
+5V
0V
+10V Vdd BT1(0)
-10V -15V WL0(0)
-10V -15V WL1(0)
-10V -15V WL31(0)
0V Vdd ST1(0)
0V 0V SL(0)
0V 0V BT1(n)
0V 0V WL0(n)
0V 0V WL1(0)
0V 0V WL31(n)
0V 0V ST1(n)
0V 0V SL(n)
T0
T1
T2
T3
Block 0
(selected)
S0
S1
S2
S3
Ma
Mb
Mc
Md
Me
Mf
Mg
Mh
Mi
Mj
Mk
Ml
B0
B1
B2
B3
T4
T5
T6
T7
T8
T9
T10
T11
Block n
(non-selected)
S4
S5
S6
S7
Mm
Mn
Mo
Mp
Mq
Mr
Ms
Mt
Mu
Mv
Mw
Mx
B4
B5
B6
B7
T12
T13
T14
T15

FIG.21

Block Erase Verify

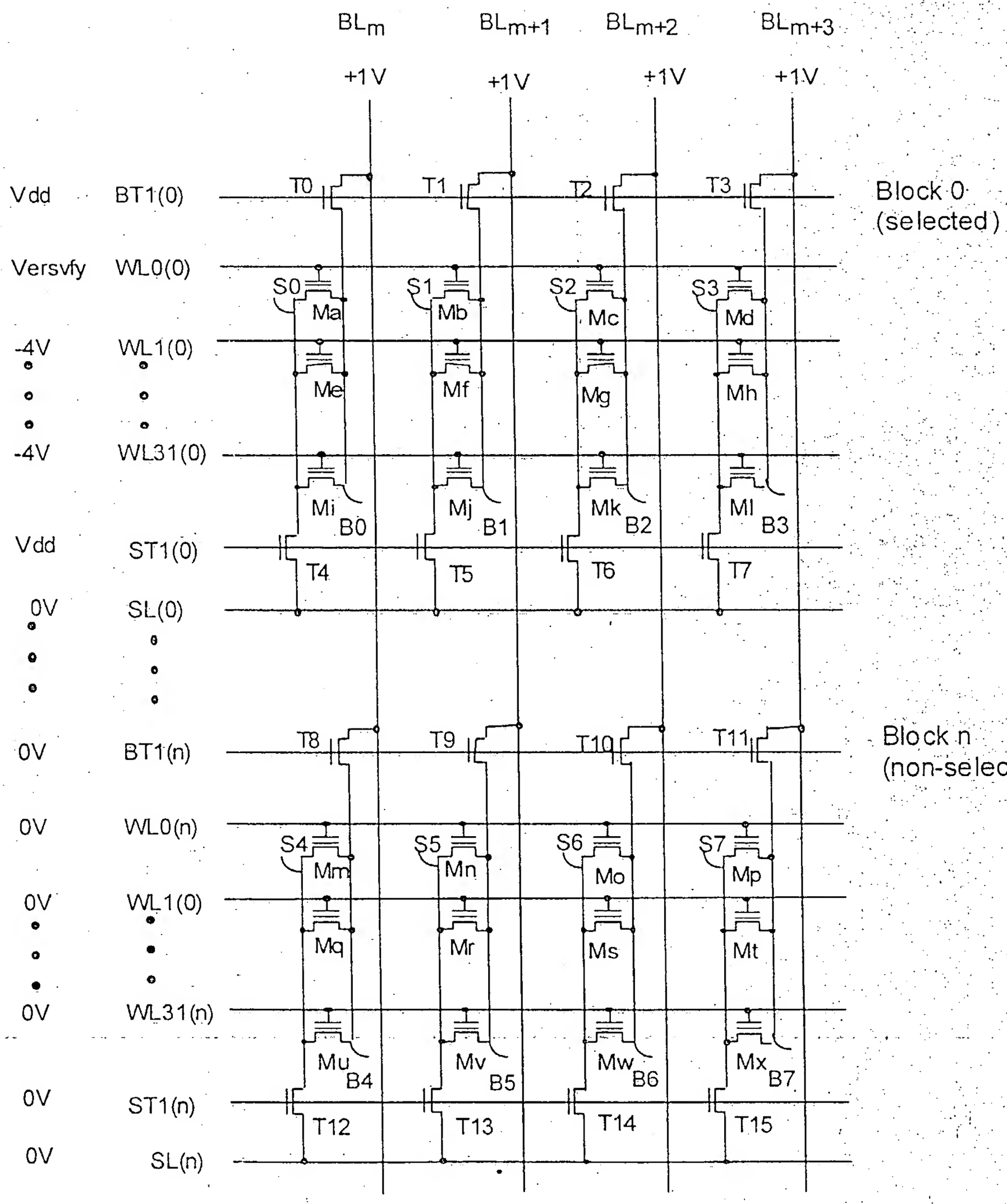


FIG. 22

Block Erase Inhibit

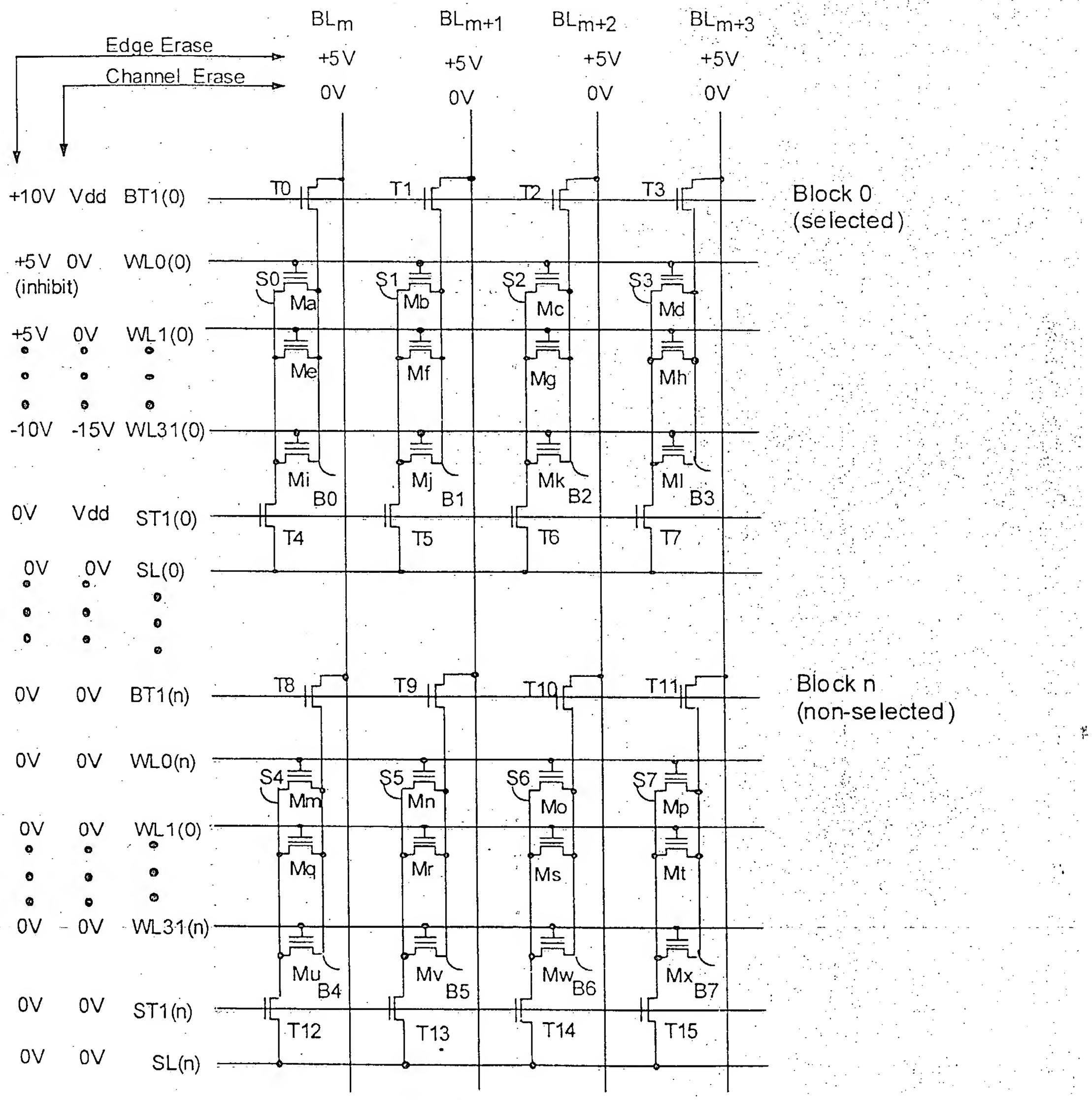


FIG. 23

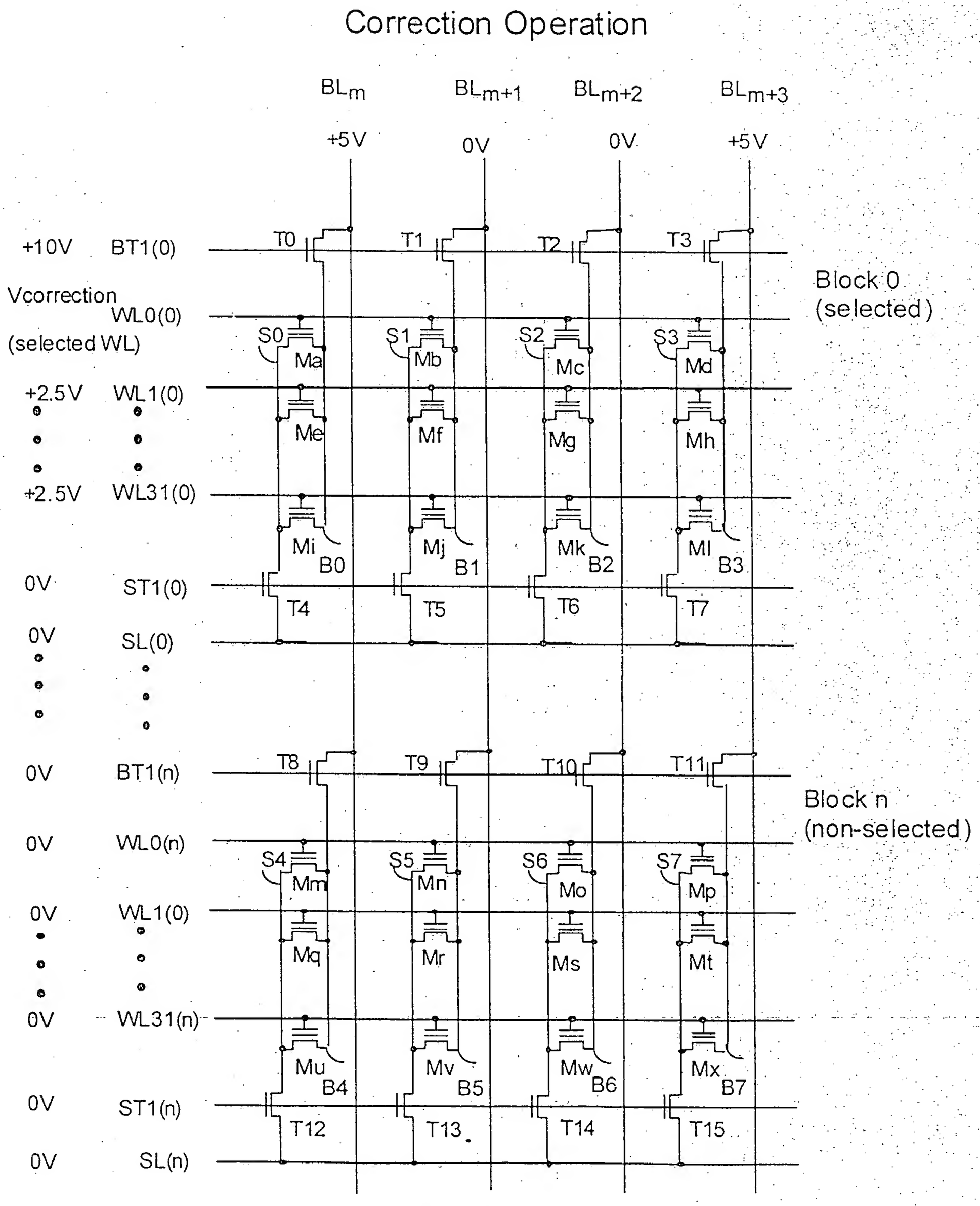

Correction Operation
BLm
BLm+1
BLm+2
BLm+3
+5V
0V
0V
+5V
+10V
BT1(0)
T0
T1
T2
T3
Block 0
(selected)
Vcorrection
WL0(0)
(selected WL)
S0
S1
S2
S3
Ma
Mb
Mc
Md
+2.5V
WL1(0)
Me
Mf
Mg
Mh
+2.5V
WL31(0)
Mi
Mj
Mk
Ml
B0
B1
B2
B3
0V
ST1(0)
T4
T5
T6
T7
0V
SL(0)
T8
T9
T10
T11
0V
BT1(n)
Block n
(non-selected)
0V
WL0(n)
S4
S5
S6
S7
Mm
Mn
Mo
Mp
0V
WL1(0)
Mq
Mr
Ms
Mt
0V
WL31(n)
Mu
Mv
Mw
Mx
B4
B5
B6
B7
0V
ST1(n)
T12
T13
T14
T15
0V
SL(n)

FIG. 24

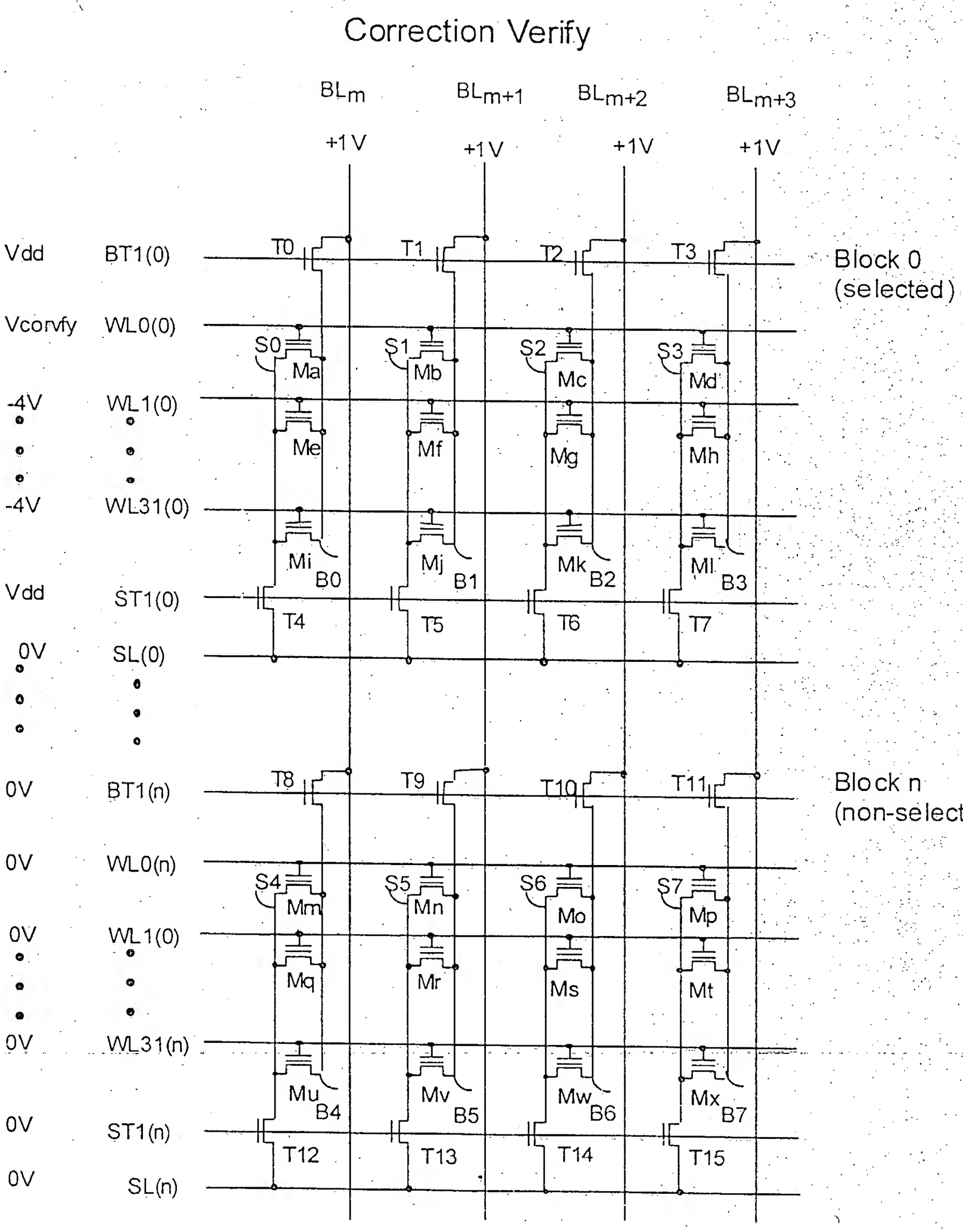

Correction Verify
BLm
BLm+1
BLm+2
BLm+3
+1V
+1V
+1V
+1V
Vdd
BT1(0)
T0
T1
T2
T3
Block 0
(selected)
Vcorvfy
WL0(0)
S0
S1
S2
S3
Ma
Mb
Mc
Md
-4V
WL1(0)
Me
Mf
Mg
Mh
-4V
WL31(0)
Mi
Mj
Mk
Ml
B0
B1
B2
B3
Vdd
ST1(0)
T4
T5
T6
T7
0V
SL(0)
0V
BT1(n)
T8
T9
T10
T11
Block n
(non-selected)
0V
WL0(n)
S4
S5
S6
S7
Mm
Mn
Mo
Mp
0V
WL1(0)
Mq
Mr
Ms
Mt
0V
WL31(n)
Mu
Mv
Mw
Mx
B4
B5
B6
B7
0V
ST1(n)
T12
T13
T14
T15
0V
SL(n)

FIG. 25

Random Page Program Operation

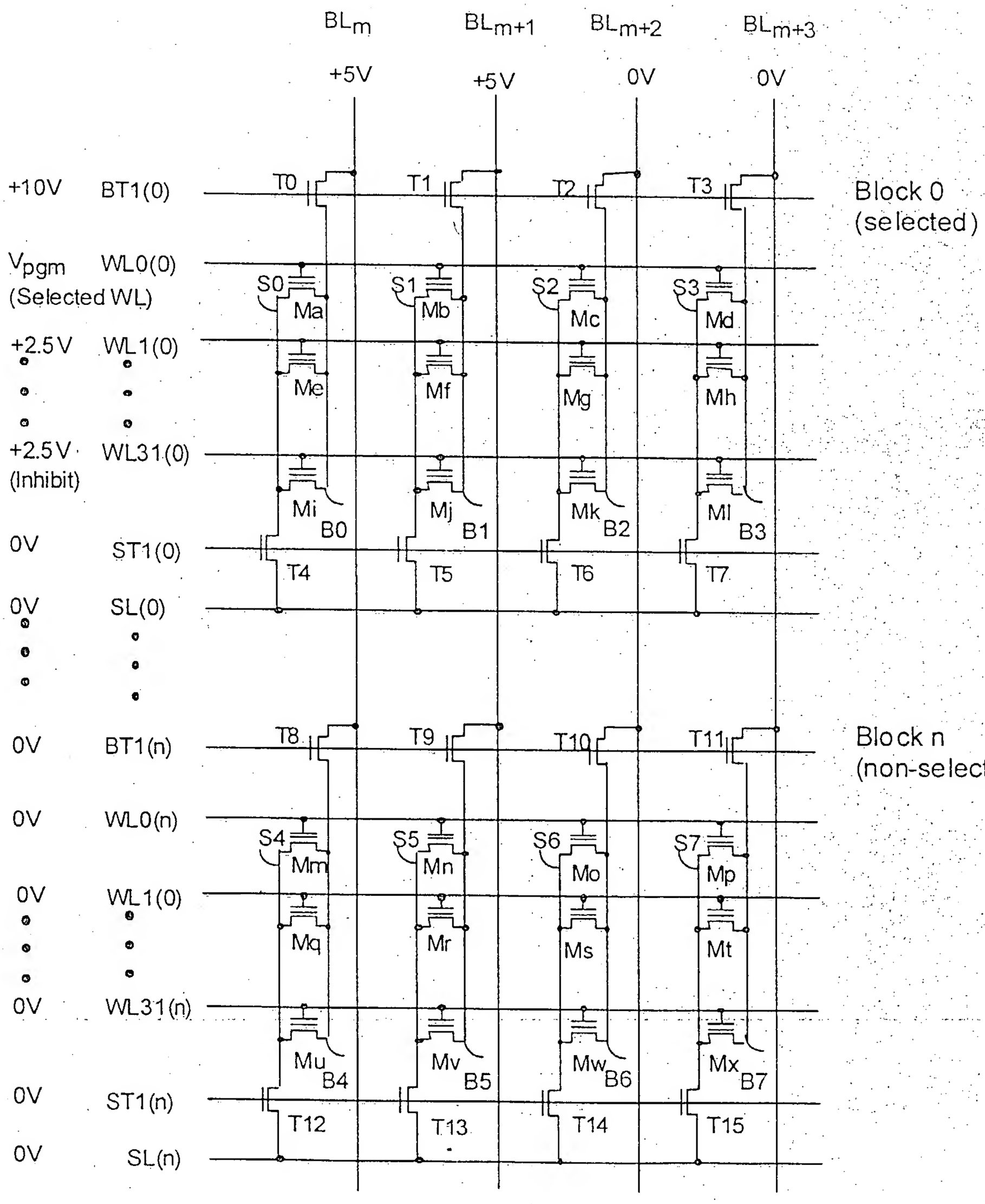


FIG. 26

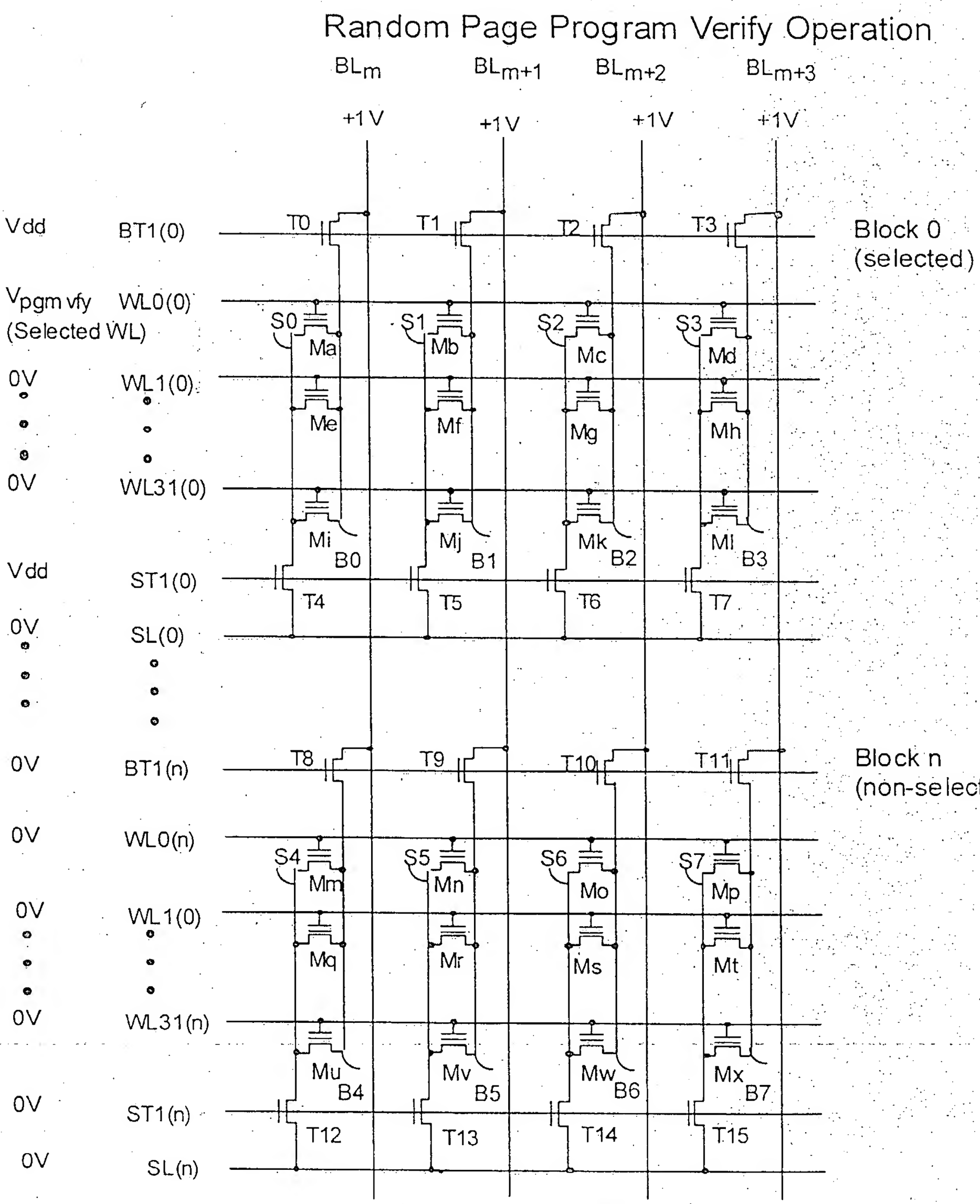
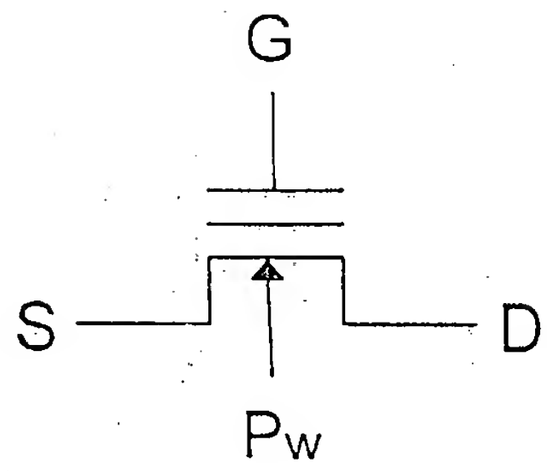

Random Page Program Verify Operation
BLm
BLm+1
BLm+2
BLm+3
+1V
+1V
+1V
+1V
Vdd
BT1(0)
T0
T1
T2
T3
Block 0
(selected)
Vpgm vfy
(Selected WL)
WL0(0)
S0
S1
S2
S3
Ma
Mb
Mc
Md
0V
WL1(0)
Me
Mf
Mg
Mh
0V
WL31(0)
Mi
Mj
Mk
Ml
B0
B1
B2
B3
Vdd
ST1(0)
T4
T5
T6
T7
0V
SL(0)
0V
BT1(n)
T8
T9
T10
T11
Block n
(non-selected)
0V
WL0(n)
S4
S5
S6
S7
Mm
Mn
Mo
Mp
0V
WL1(0)
Mq
Mr
Ms
Mt
0V
WL31(n)
Mu
Mv
Mw
Mx
B4
B5
B6
B7
0V
ST1(n)
T12
T13
T14
T15
0V
SL(n)

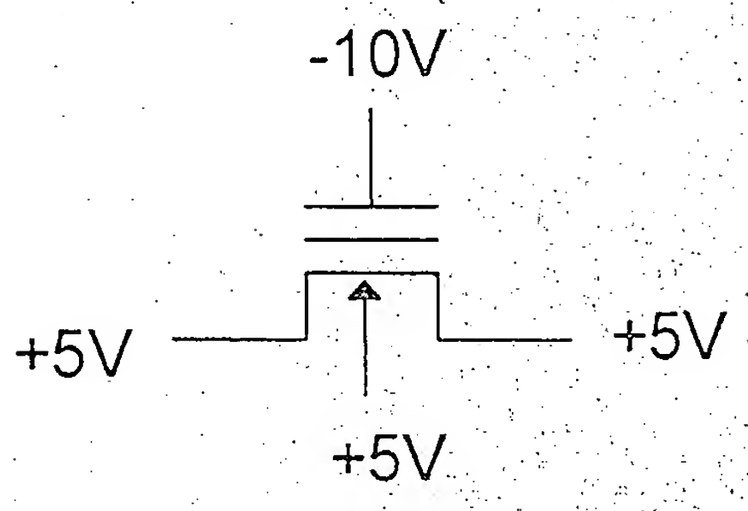
FIG. 27

ETOX NOR cell on a P-well

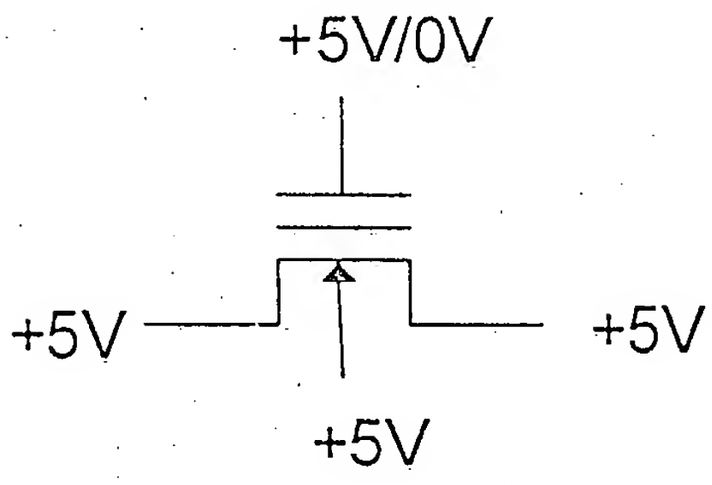
a)



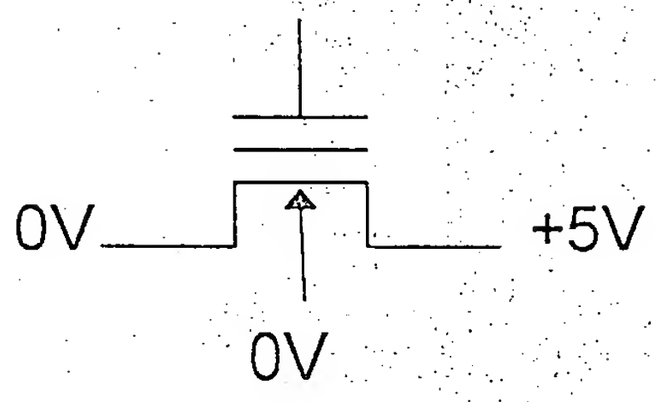
b) ERASE



c) ERASE INHIBIT



d) CORRECTION



e) PROGRAM

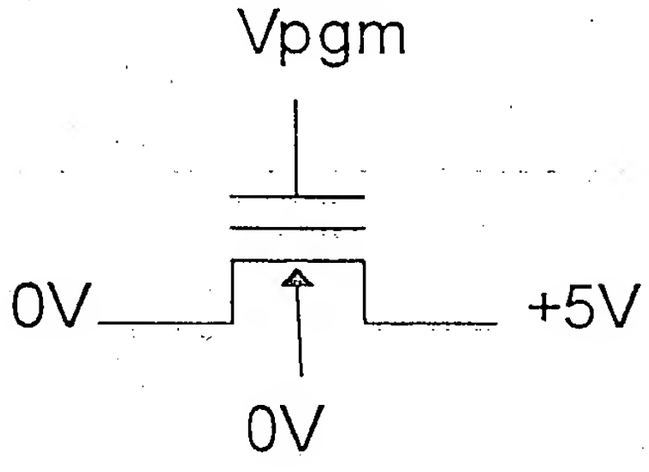


FIG. 28

ETOX NOR cell on a P-well

a)

Vpgmvfy

0V

+1V

0V

b) CORRECTION VERIFY

Vcorvfy

0V

+1V

0V

c) READ

Vread

0V

+1V

0V

d) ERASE VERIFY

Versvfy

0V

+1V

0V

FIG. 29

ETOX NOR Array on a Pwell

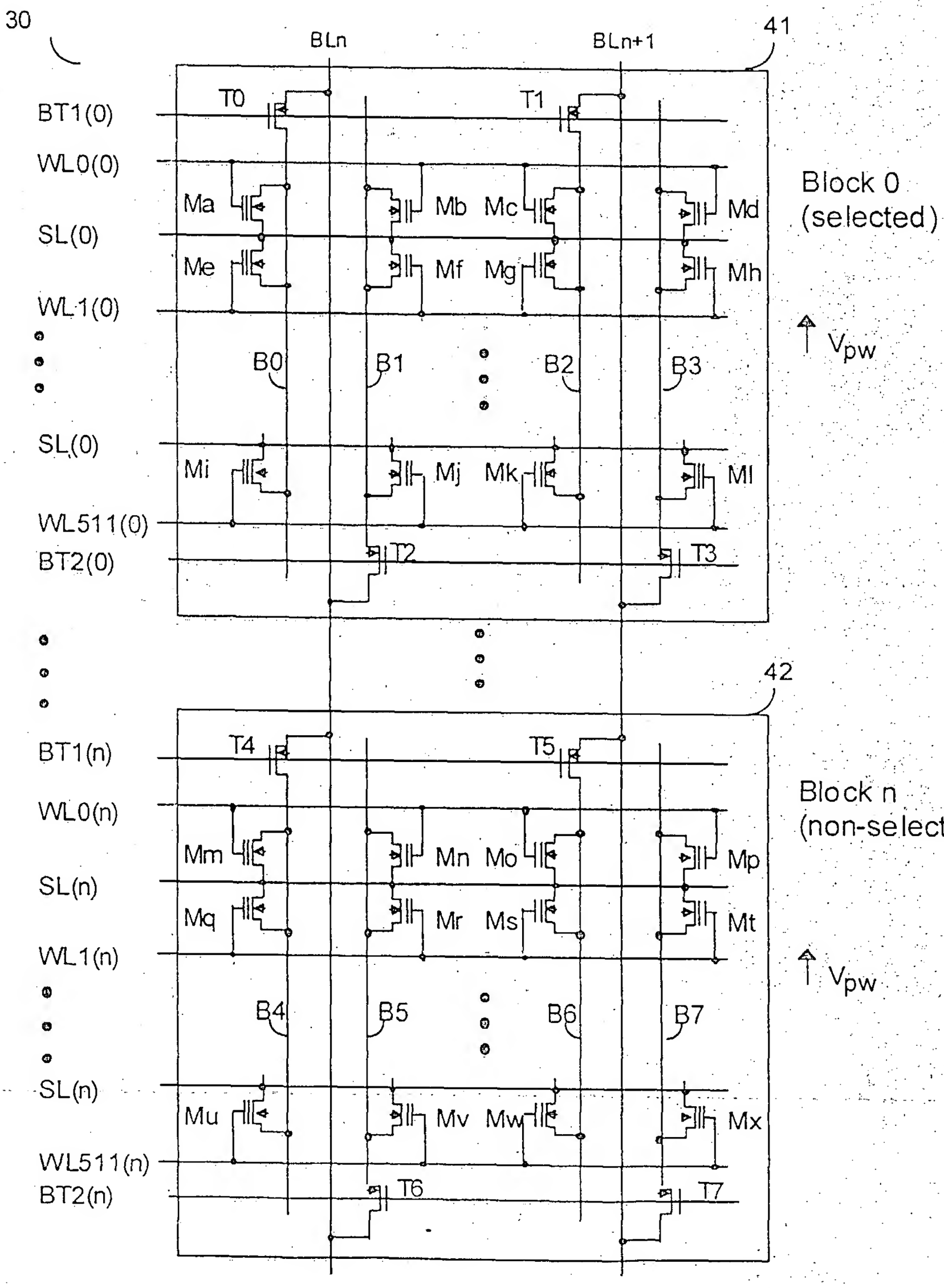


FIG. 30

Block Erase Operations

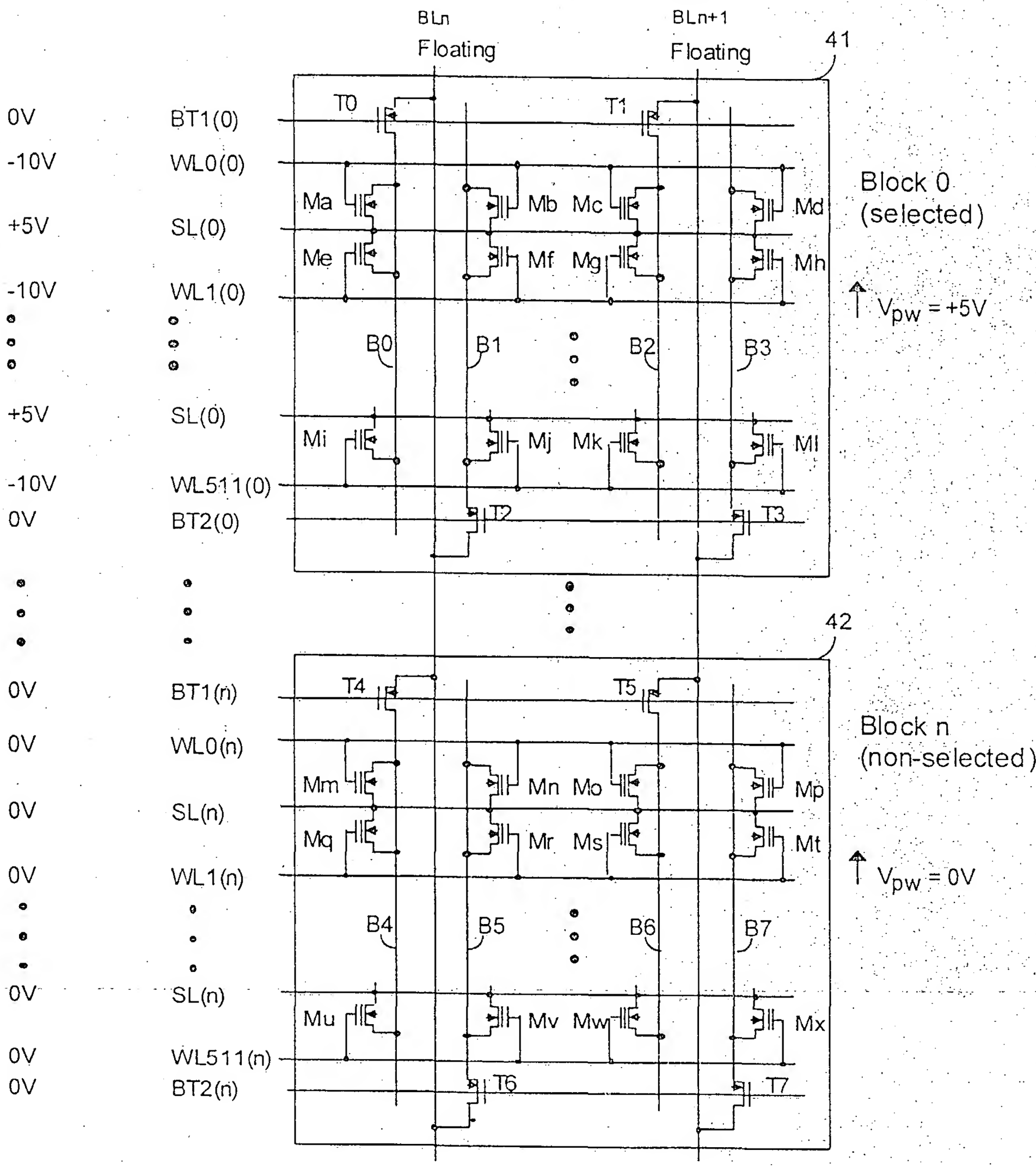


FIG. 31

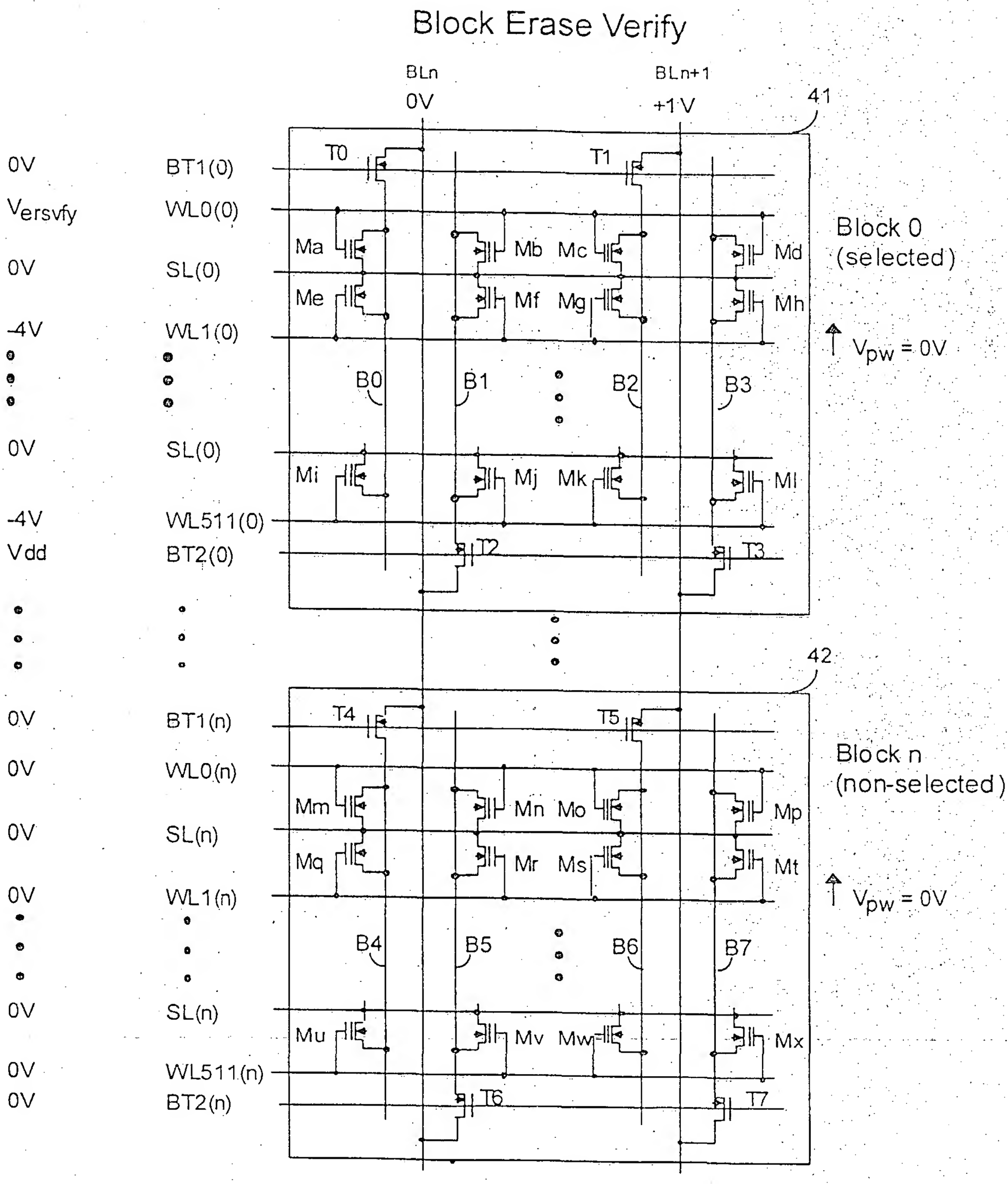

Block Erase Verify
BLn
0V
BLn+1
+1V
41
0V
BT1(0)
Versvfy
WL0(0)
0V
SL(0)
-4V
WL1(0)
0V
SL(0)
-4V
WL511(0)
Vdd
BT2(0)
T0
T1
Ma
Mb
Mc
Md
Me
Mf
Mg
Mh
B0
B1
B2
B3
Mi
Mj
Mk
Ml
T2
T3
Block 0
(selected)
Vpw = 0V
42
0V
BT1(n)
0V
WL0(n)
0V
SL(n)
0V
WL1(n)
0V
SL(n)
0V
WL511(n)
0V
BT2(n)
T4
T5
Mm
Mn
Mo
Mp
Mq
Mr
Ms
Mt
B4
B5
B6
B7
Mu
Mv
Mw
Mx
T6
T7
Block n
(non-selected)
Vpw = 0V

FIG. 32

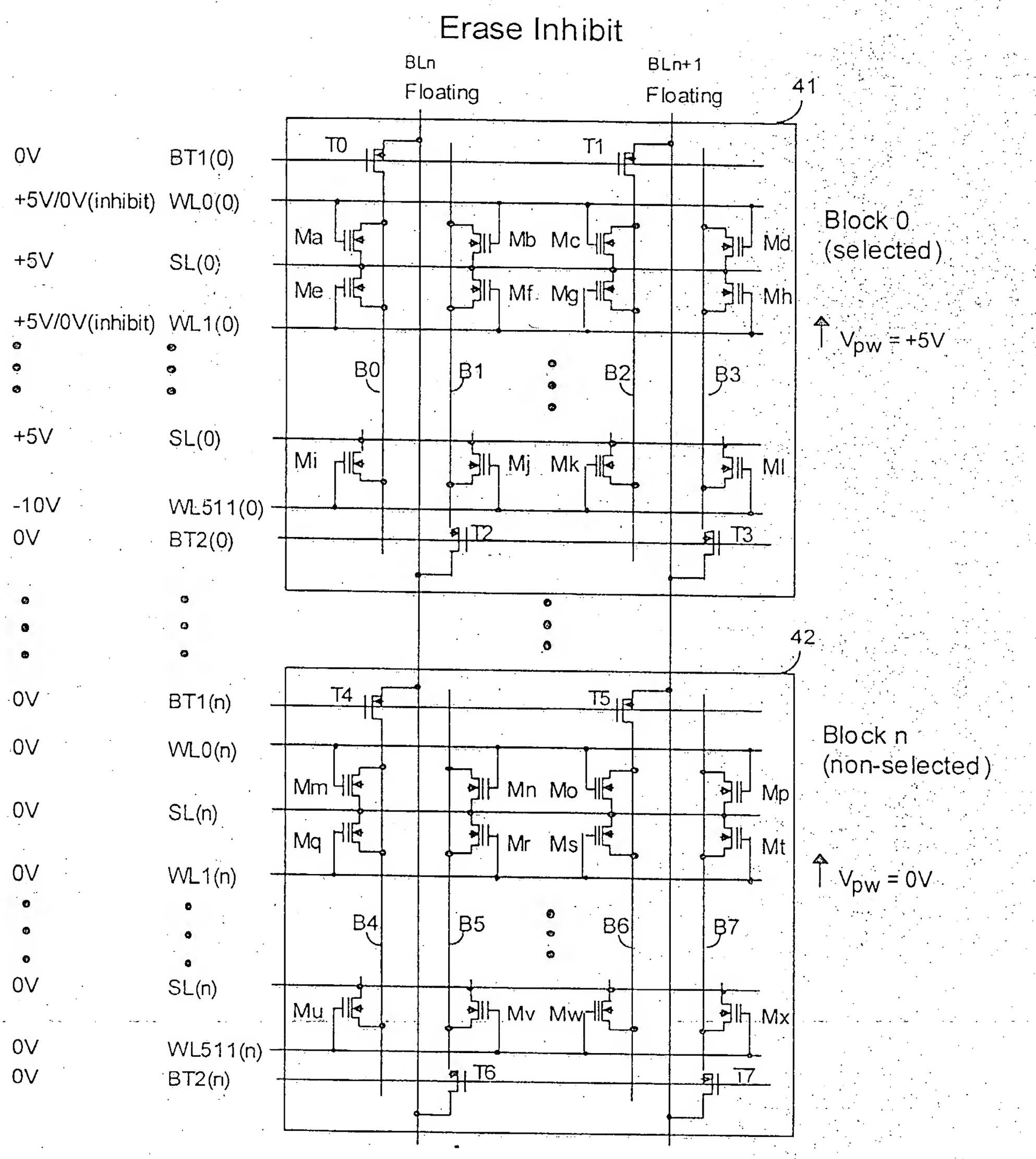

Erase Inhibit
BLn
Floating
BLn+1
Floating
41
0V
BT1(0)
+5V/0V(inhibit)
WL0(0)
+5V
SL(0)
+5V/0V(inhibit)
WL1(0)
+5V
SL(0)
-10V
WL511(0)
0V
BT2(0)
T0
T1
Ma
Mb
Mc
Md
Me
Mf
Mg
Mh
B0
B1
B2
B3
Mi
Mj
Mk
Ml
T2
T3
Block 0
(selected)
V_{pw} = +5V
42
0V
BT1(n)
0V
WL0(n)
0V
SL(n)
0V
WL1(n)
0V
SL(n)
0V
WL511(n)
0V
BT2(n)
T4
T5
Mm
Mn
Mo
Mp
Mq
Mr
Ms
Mt
B4
B5
B6
B7
Mu
Mv
Mw
Mx
T6
T7
Block n
(non-selected)
V_{pw} = 0V

FIG. 33

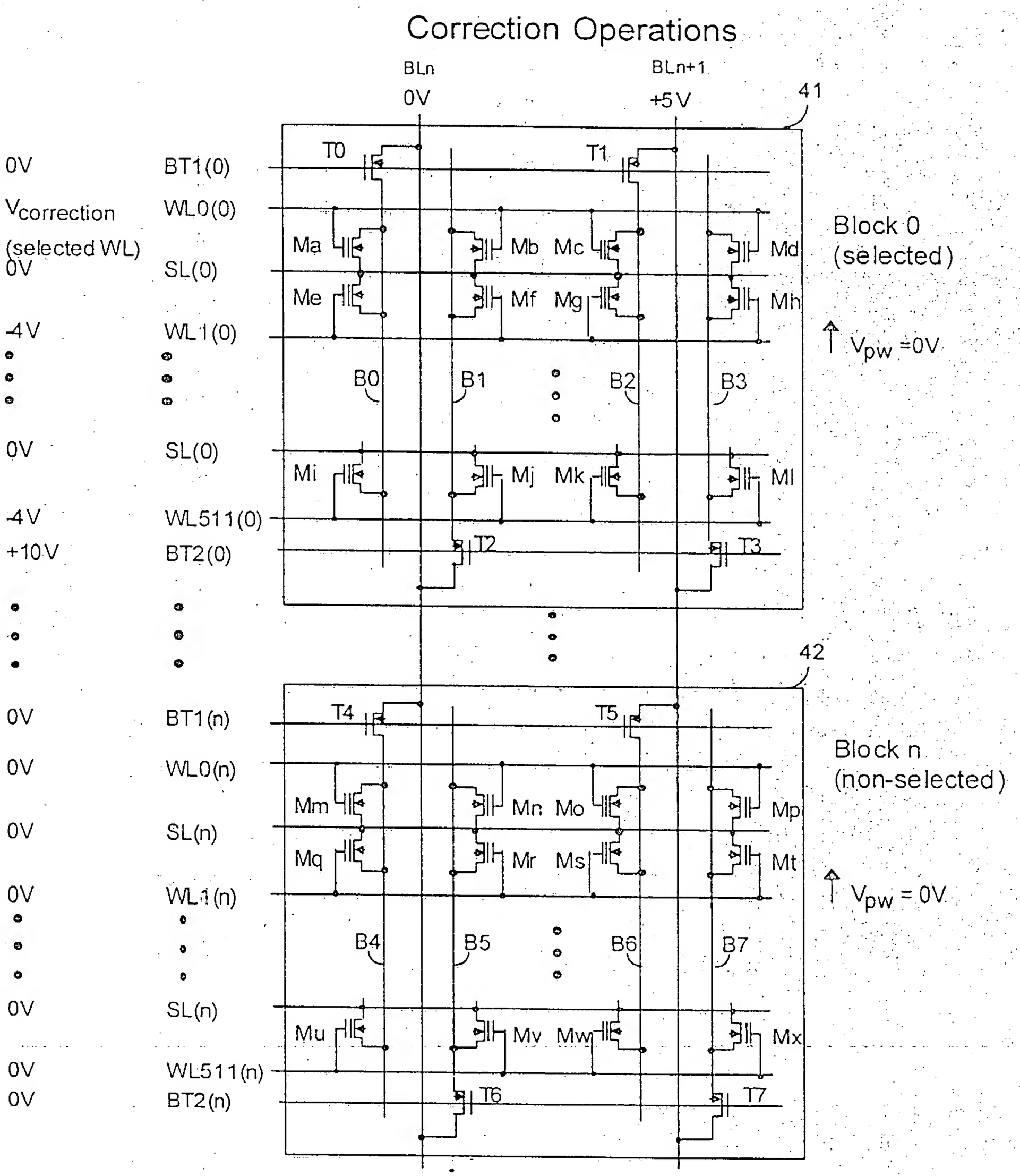

Correction Operations
BLn
0V
BLn+1
+5V
41
T0
T1
0V
BT1(0)
Vcorrection
(selected WL)
WL0(0)
0V
SL(0)
Ma
Mb
Mc
Md
Me
Mf
Mg
Mh
Block 0
(selected)
-4V
WL1(0)
Vpw =0V
B0
B1
B2
B3
0V
SL(0)
Mi
Mj
Mk
Ml
-4V
WL511(0)
+10V
BT2(0)
T2
T3
42
0V
BT1(n)
T4
T5
0V
WL0(n)
Mm
Mn
Mo
Mp
0V
SL(n)
Mq
Mr
Ms
Mt
Block n
(non-selected)
0V
WL1(n)
Vpw = 0V
B4
B5
B6
B7
0V
SL(n)
Mu
Mv
Mw
Mx
0V
WL511(n)
0V
BT2(n)
T6
T7

FIG. 34

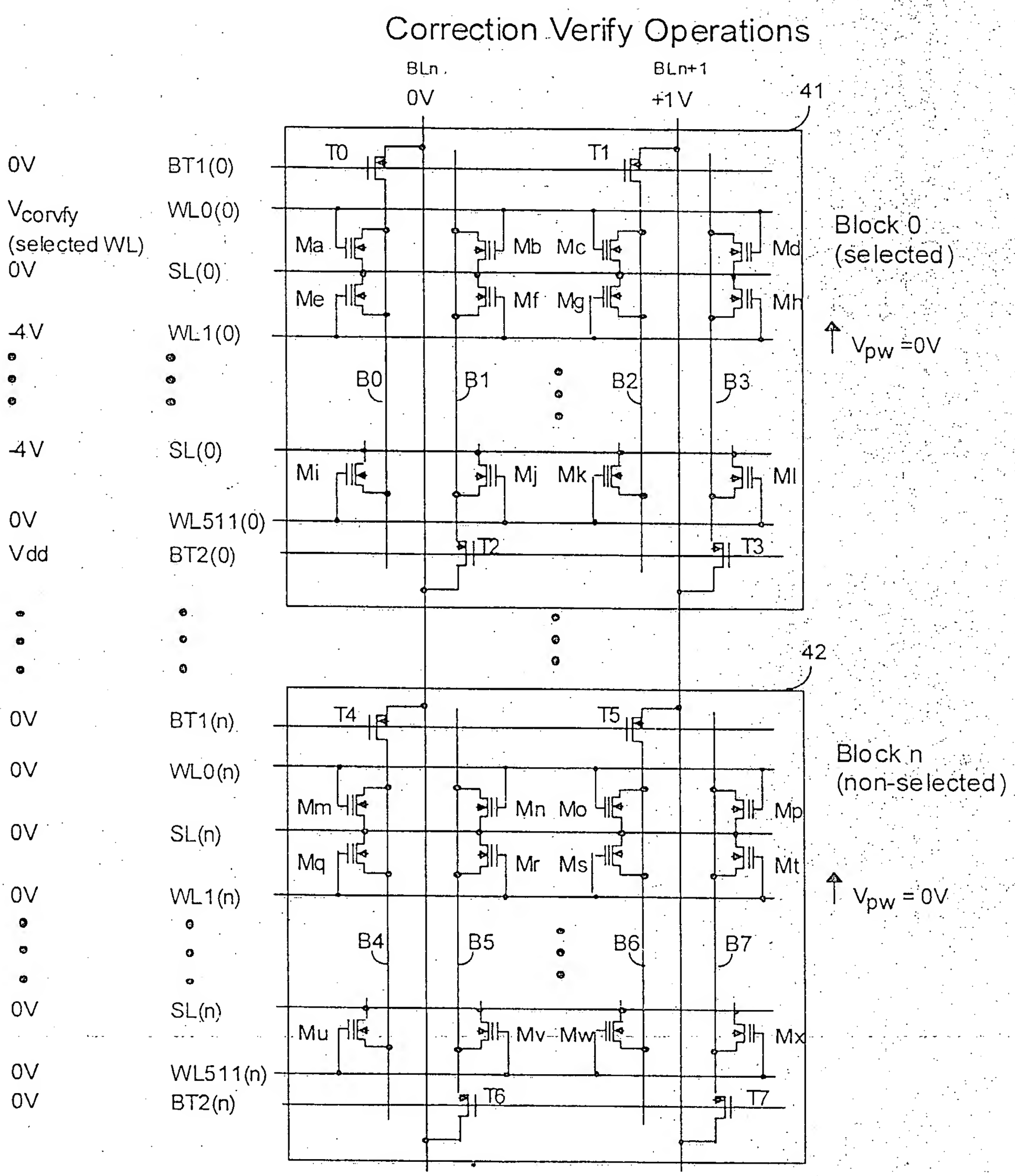

Correction Verify Operations
BLn
0V
BLn+1
+1V
41
0V
BT1(0)
T0
T1
Vcorvfy
(selected WL)
WL0(0)
Ma
Mb
Mc
Md
Block 0
(selected)
0V
SL(0)
Me
Mf
Mg
Mh
-4V
WL1(0)
Vpw =0V
B0
B1
B2
B3
-4V
SL(0)
Mi
Mj
Mk
Ml
0V
WL511(0)
Vdd
BT2(0)
T2
T3
42
0V
BT1(n)
T4
T5
0V
WL0(n)
Mm
Mn
Mo
Mp
Block n
(non-selected)
0V
SL(n)
Mq
Mr
Ms
Mt
0V
WL1(n)
Vpw = 0V
B4
B5
B6
B7
0V
SL(n)
Mu
Mv
Mw
Mx
0V
WL511(n)
0V
BT2(n)
T6
T7

FIG.35

Program Operations

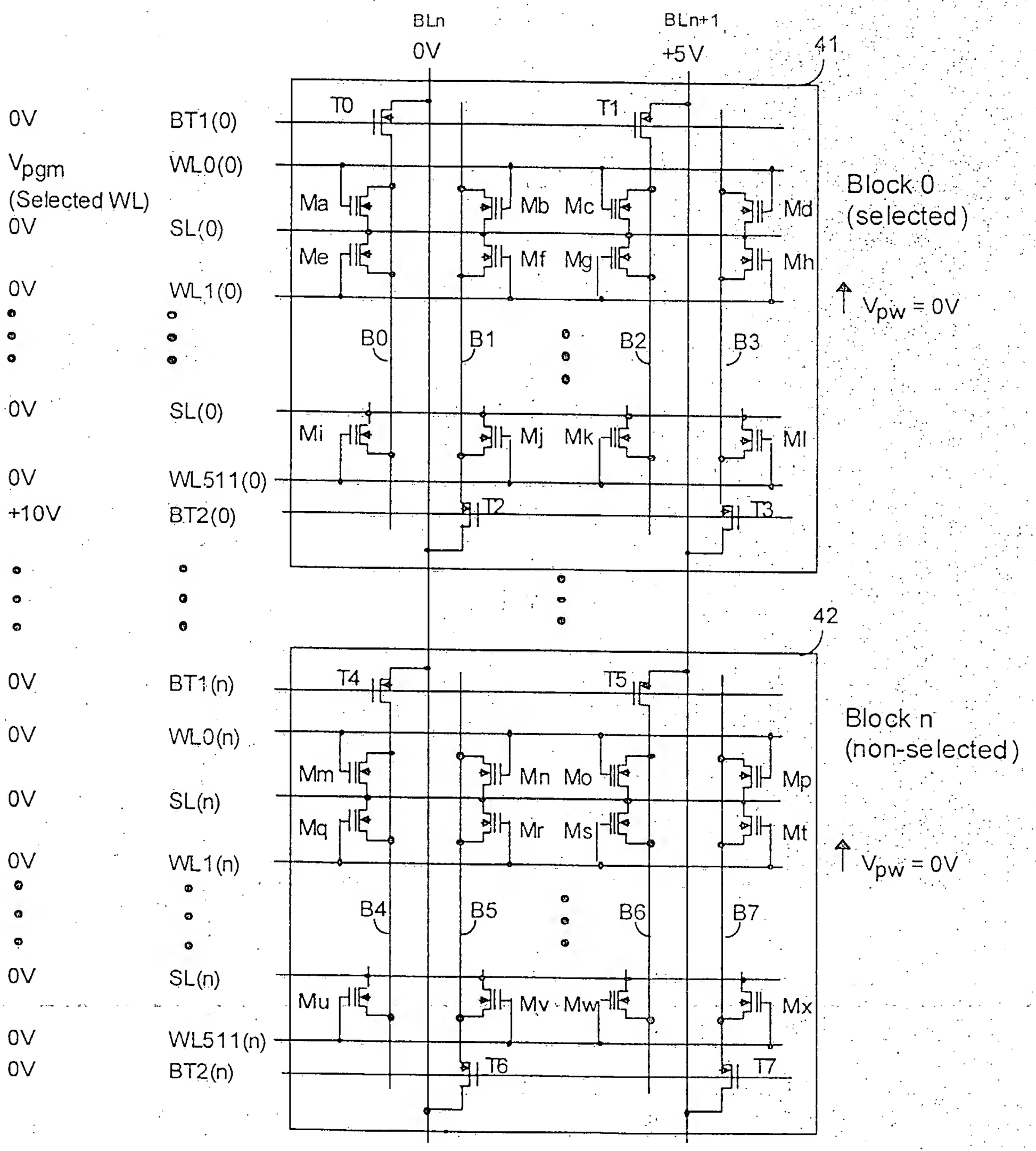


FIG. 36

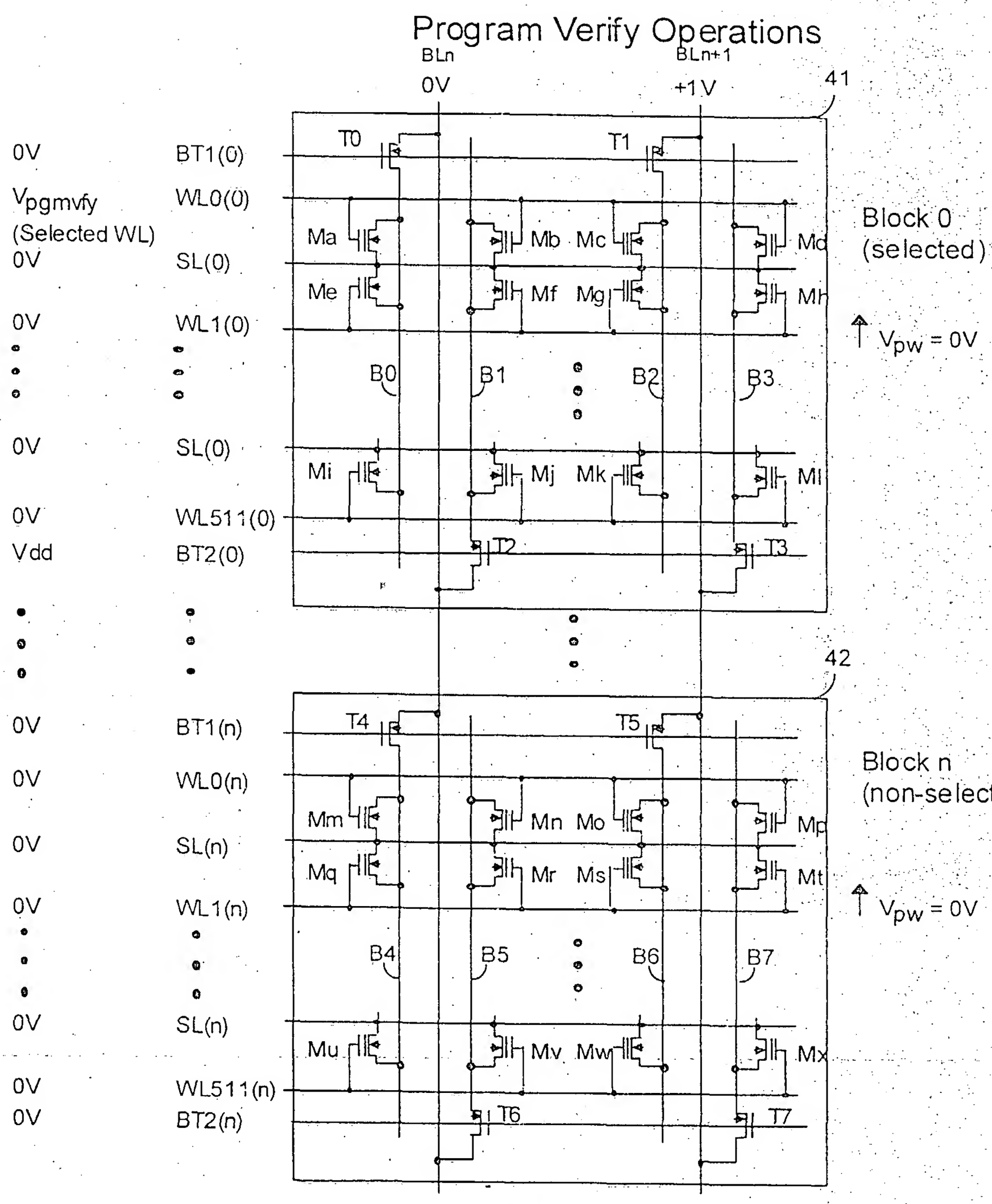

Program Verify Operations
BLn
BLn+1
0V
+1V
41
T0
T1
0V
BT1(0)
V_{pgmvfy}
WL0(0)
(Selected WL)
0V
SL(0)
Ma
Mb
Mc
Md
Me
Mf
Mg
Mh
Block 0
(selected)
0V
WL1(0)
V_{pw} = 0V
B0
B1
B2
B3
0V
SL(0)
Mi
Mj
Mk
Ml
0V
WL511(0)
Vdd
BT2(0)
T2
T3
42
T4
T5
0V
BT1(n)
0V
WL0(n)
Mm
Mn
Mo
Mp
0V
SL(n)
Mq
Mr
Ms
Mt
Block n
(non-selected)
0V
WL1(n)
V_{pw} = 0V
B4
B5
B6
B7
0V
SL(n)
Mu
Mv
Mw
Mx
0V
WL511(n)
0V
BT2(n)
T6
T7

FIG. 37

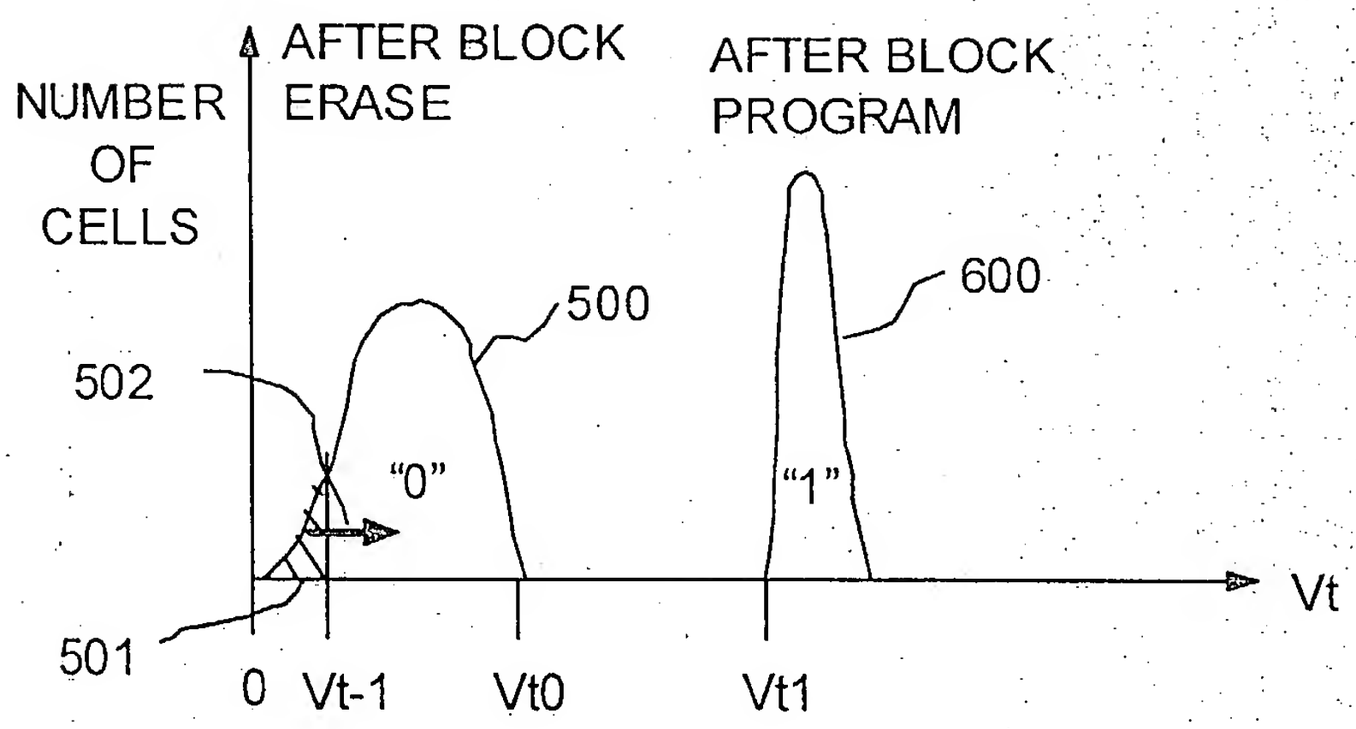


FIG.38a (Prior Art)

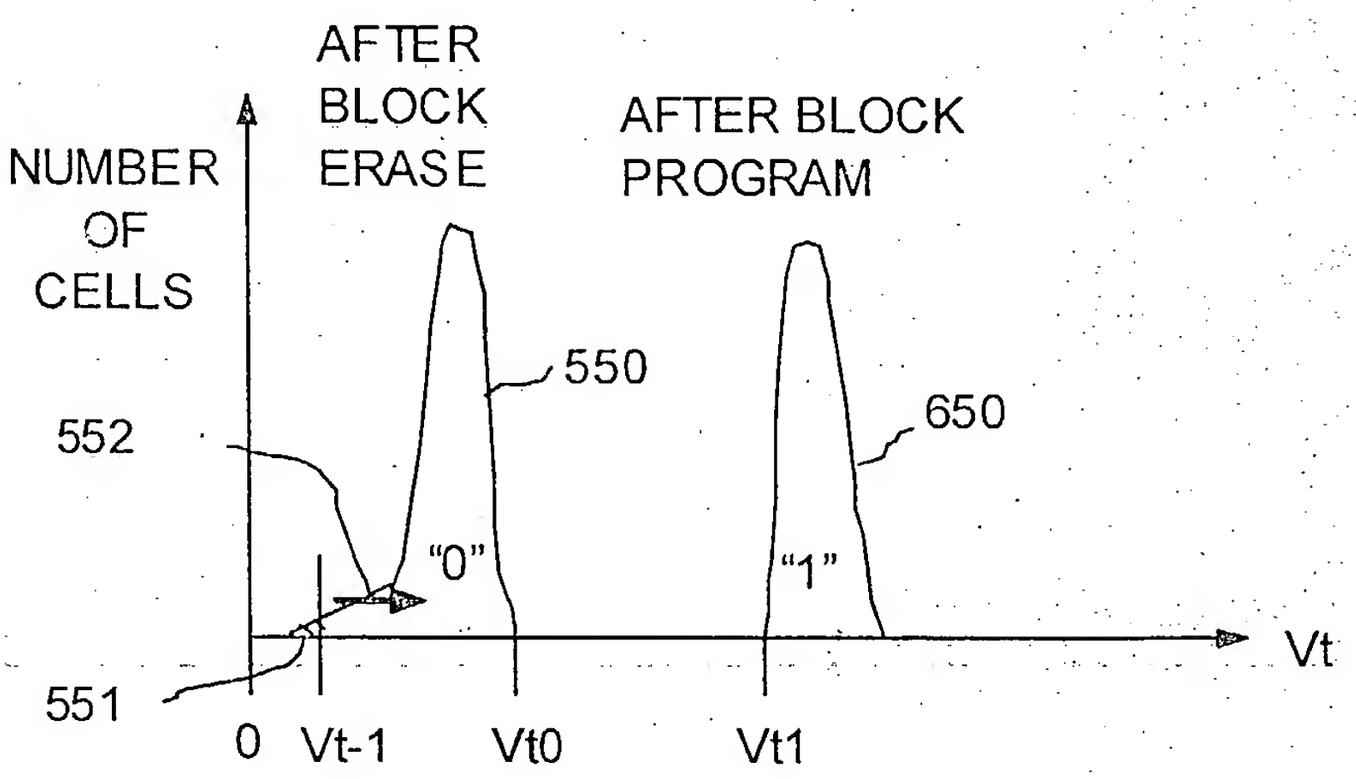


FIG.38b

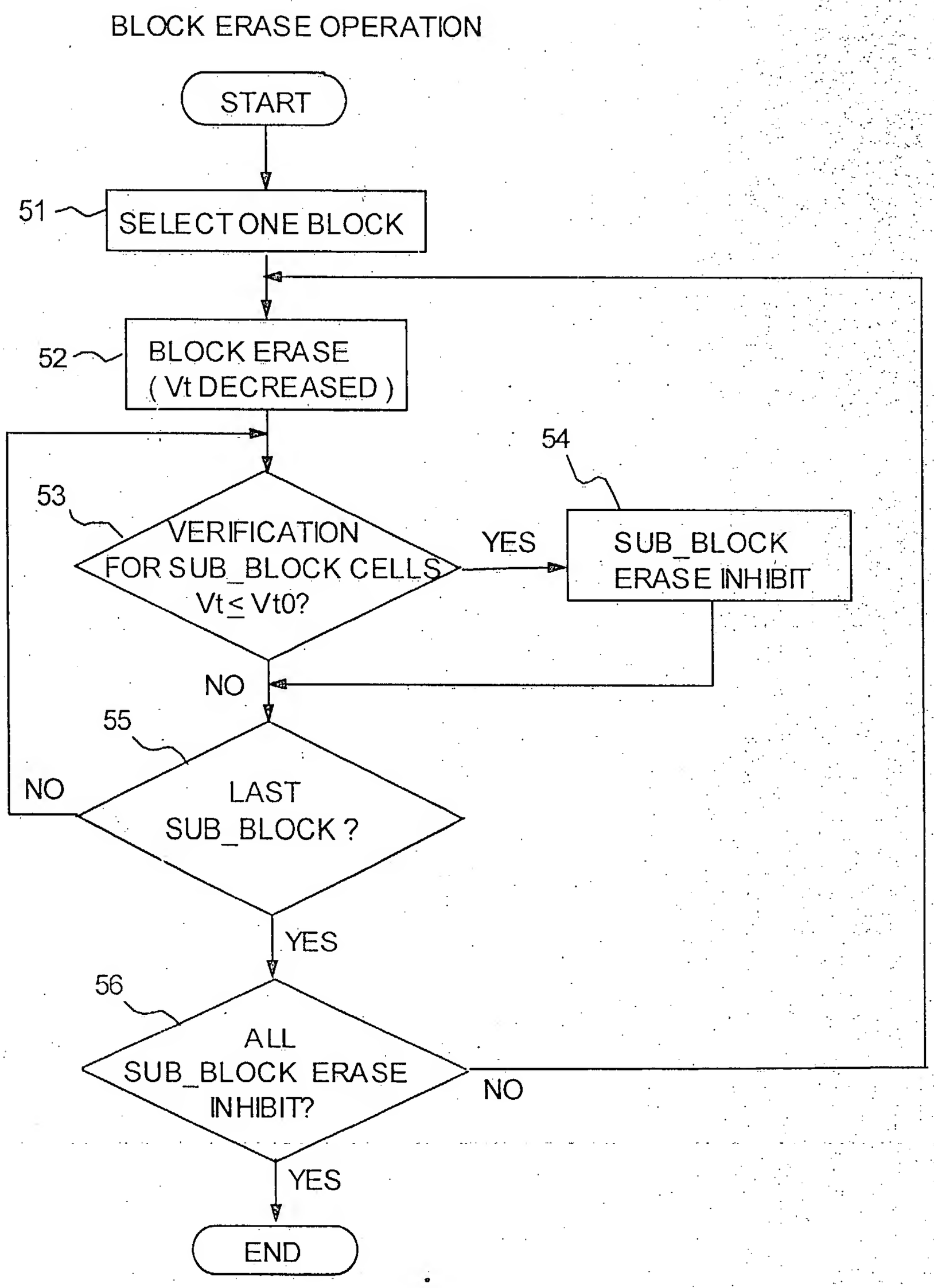

BLOCK ERASE OPERATION
START
51
SELECT ONE BLOCK
52
BLOCK ERASE
(Vt DECREASED)
53
VERIFICATION
FOR SUB_BLOCK CELLS
Vt ≤ Vt0?
YES
54
SUB_BLOCK
ERASE INHIBIT
NO
55
LAST
SUB_BLOCK ?
NO
YES
56
ALL
SUB_BLOCK ERASE
INHIBIT?
NO
YES
END

FIG. 39

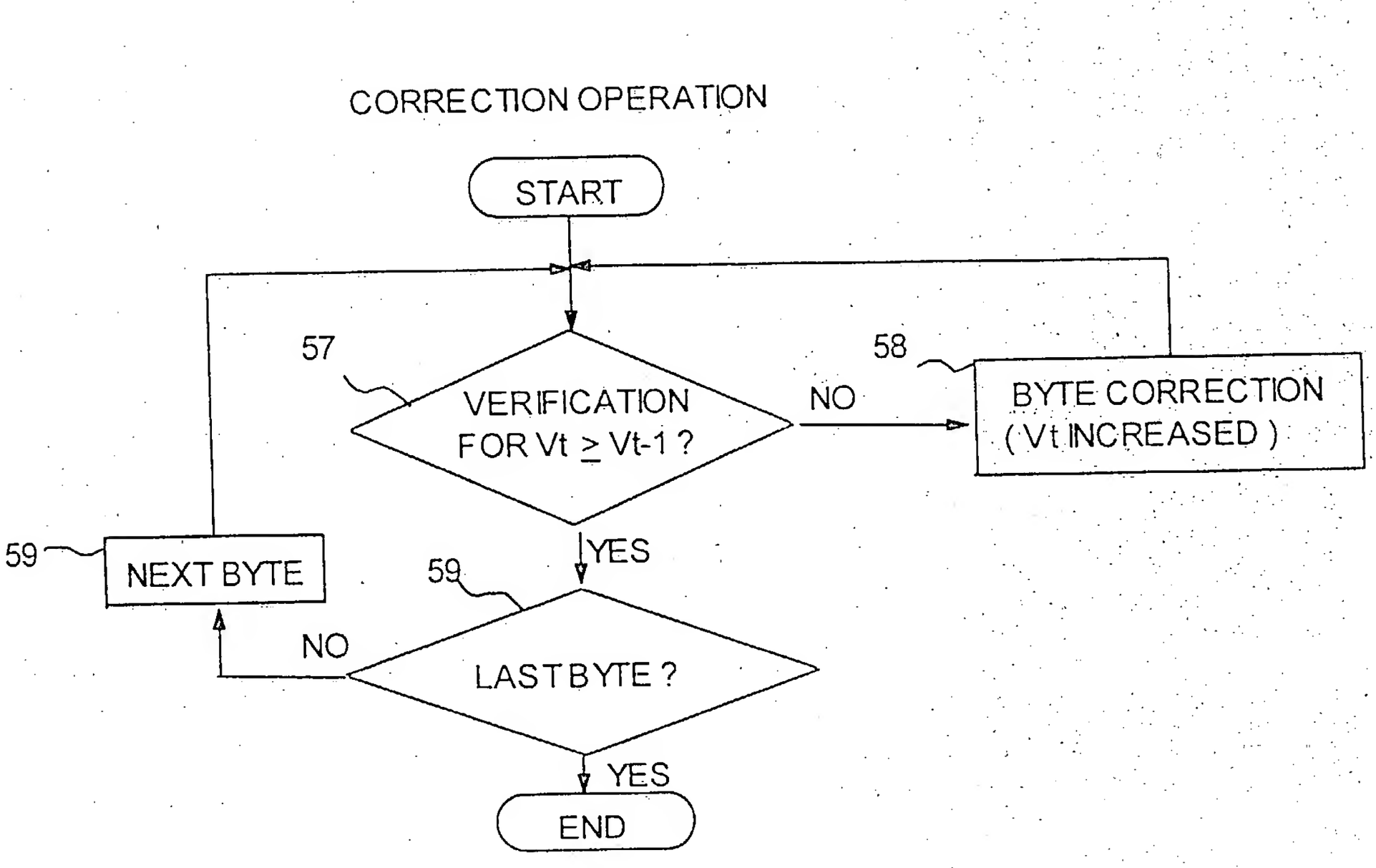

CORRECTION OPERATION
START
57
VERIFICATION FOR Vt ≥ Vt-1 ?
NO
58
BYTE CORRECTION (Vt INCREASED)
YES
59
NEXT BYTE
59
NO
LAST BYTE ?
YES
END

FIG. 40

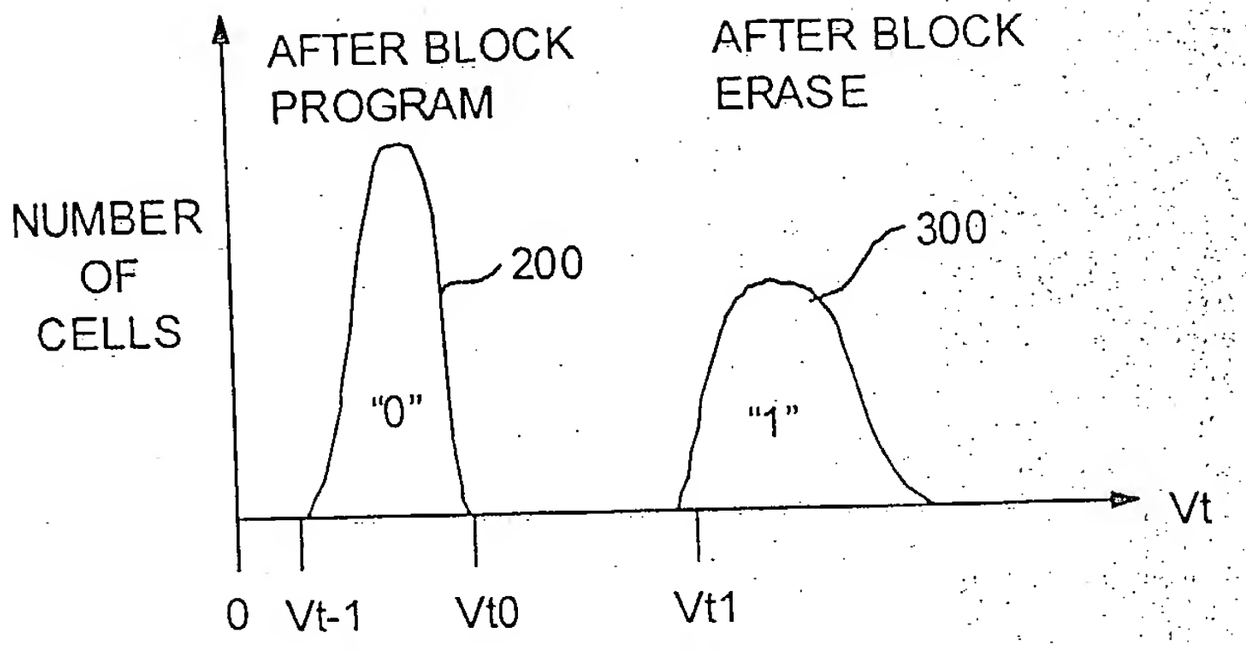


FIG.41a (Prior Art)

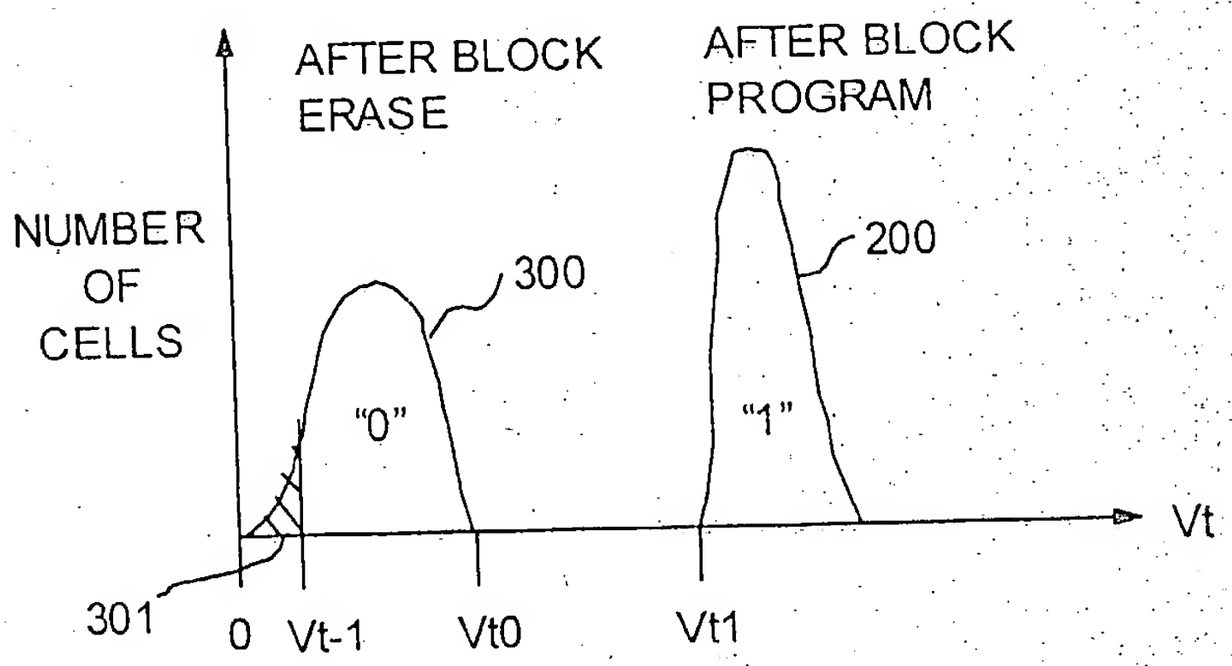


FIG.41b (Prior Art)

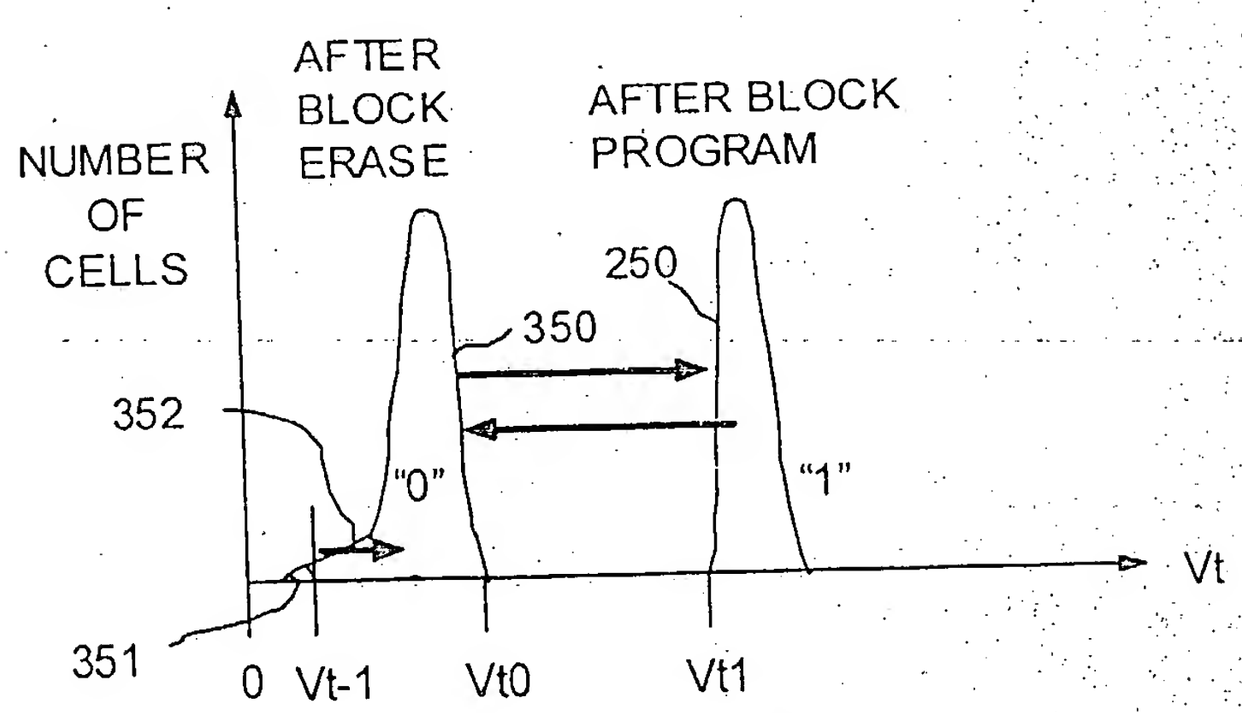


FIG.41c

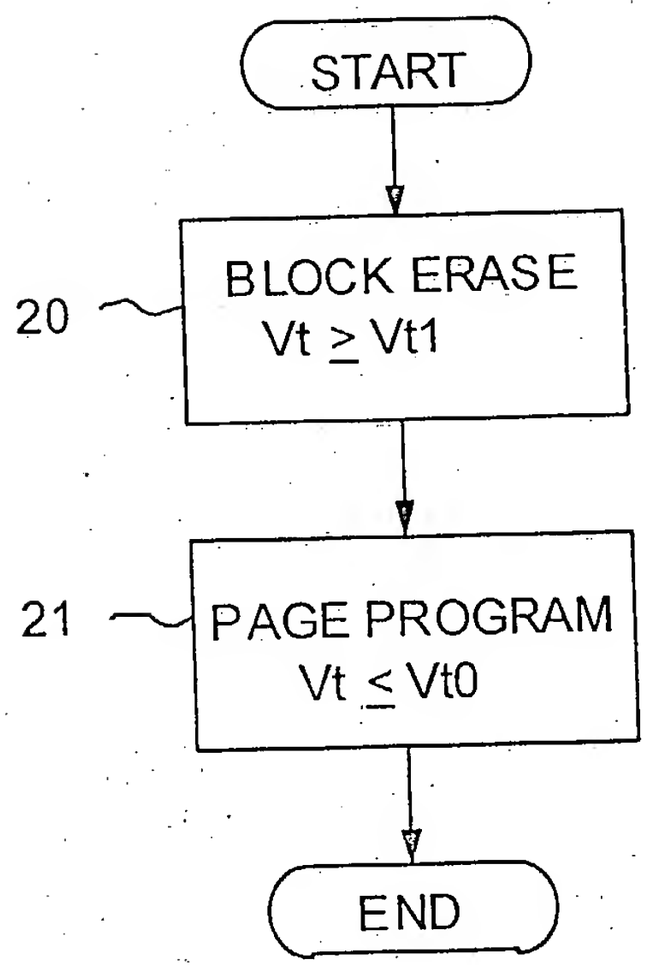


FIG.42a
(Prior Art)

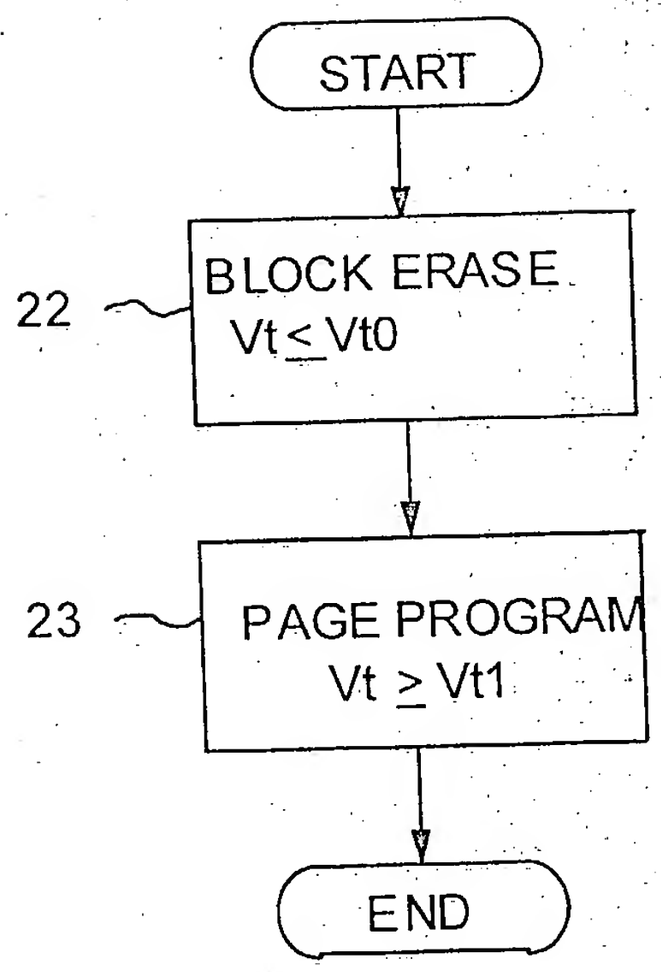


FIG.42b
(Prior Art)

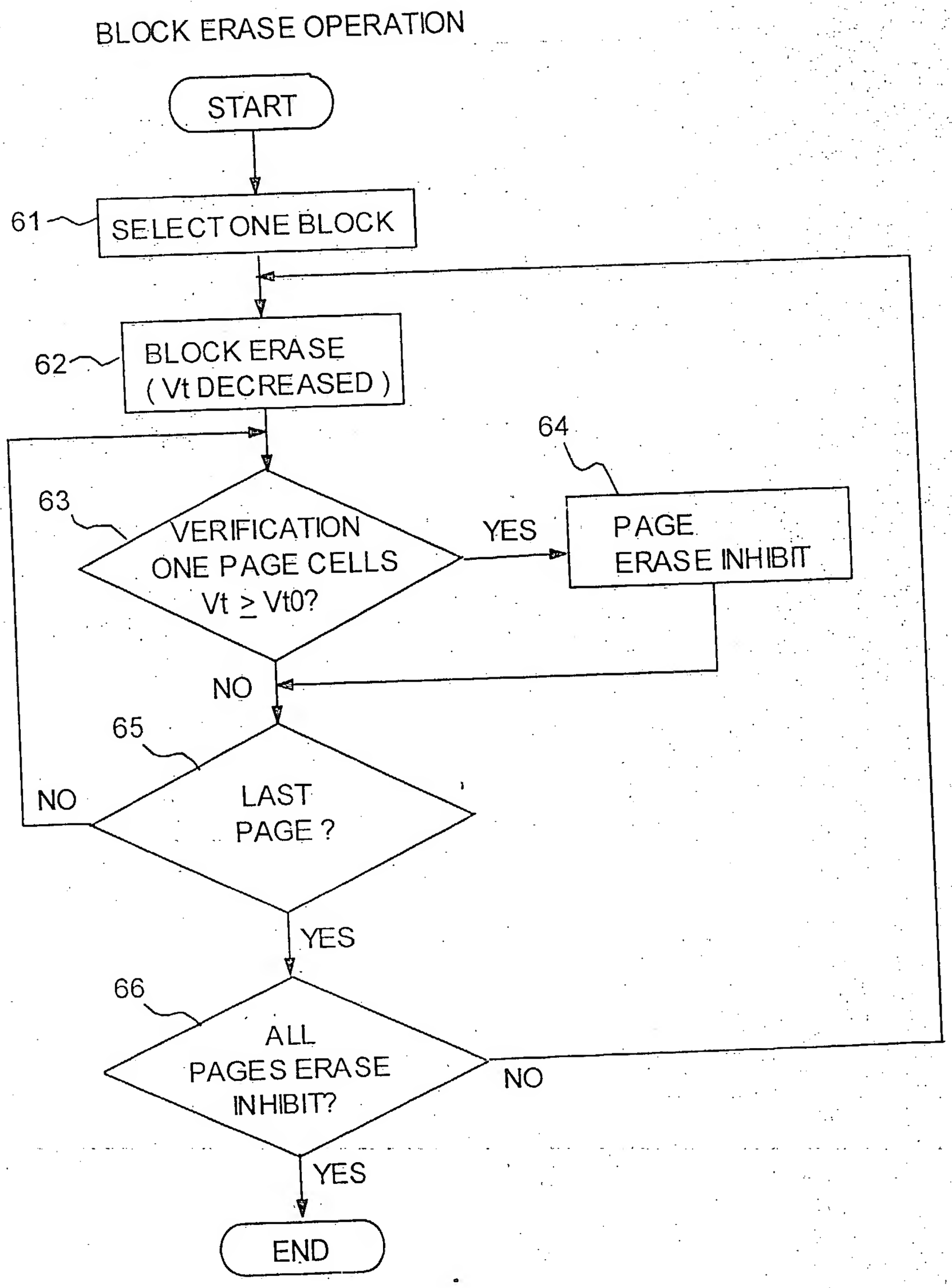

BLOCK ERASE OPERATION
START
61
SELECT ONE BLOCK
62
BLOCK ERASE
(Vt DECREASED)
63
VERIFICATION
ONE PAGE CELLS
Vt ≥ Vt0?
YES
64
PAGE
ERASE INHIBIT
NO
65
LAST
PAGE ?
NO
YES
66
ALL
PAGES ERASE
INHIBIT?
NO
YES
END

FIG. 43

CORRECTION OPERATION

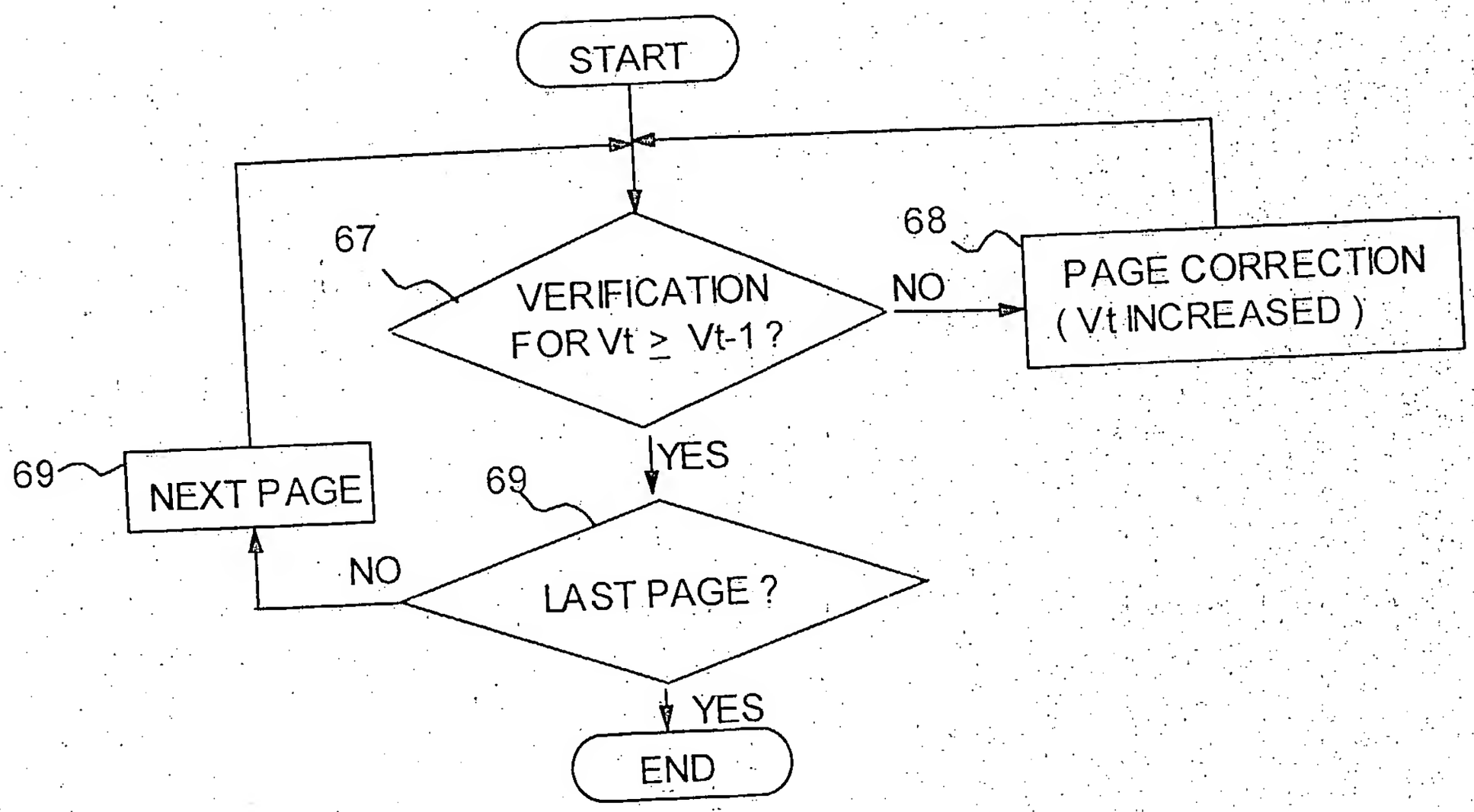


FIG. 44